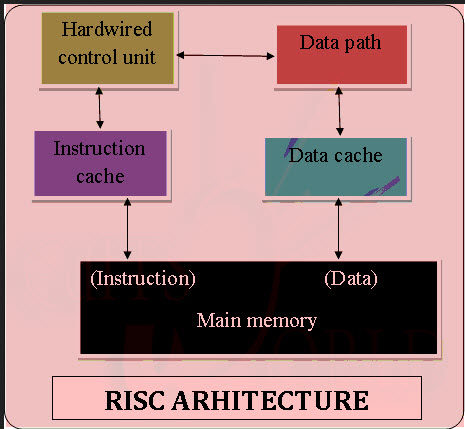
Briefly explain each of the following architectures: 1. RISC 2. CISC 3. VLIW.

Solution

1. RISC: RISC, or Reduced Instruction Set Computer. is a type of microprocessor architecture that utilizes a small, highly-optimized set of instructions, rather than a more specialized set of instructions often found in other types of architectures. RISC (Reduced Instruction Set Computer) is used in portable devices due to its power efficiency. For Example, Apple iPod and Nintendo DS. RISC is a type of microprocessor architecture that uses highly-optimized set of instructions. RISC does the opposite, reducing the cycles per instruction at the cost of the number of instructions per program Pipelining is one of the unique feature of RISC. It is performed by overlapping the execution of several instructions in a pipeline fashion. It has a high performance advantage over CISC.

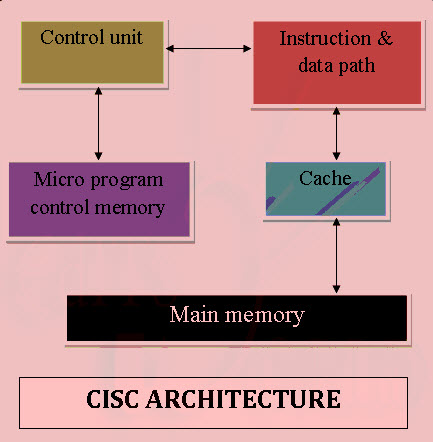


RISC processors take simple instructions and are executed within a clock cycle

#### RISC ARCHITECTURE CHARACTERISTICS

* Simple Instructions are used in RISC architecture.
* RISC helps and supports few simple data types and synthesize complex data types.
* RISC utilizes simple addressing modes and fixed length instructions for pipelining.
* RISC permits any register to use in any context.
* One Cycle Execution Time
* The amount of work that a computer can perform is reduced by separating “LOAD” and “STORE” instructions.
* RISC contains Large Number of Registers in order to prevent various number of interactions with memory.
* In RISC, Pipelining is easy as the execution of all instructions will be done in  a uniform interval of time i.e. one click.
* In RISC, more RAM is required to store assembly level instructions.
* Reduced instructions need a less number of transistors in RISC.
* RISC uses Harvard memory model means it is Harvard Architecture.
* A compiler is used to perform the conversion operation means to convert a high-level language statement into the code of its form.

1. CISC: CISC has the ability to execute addressing modes or multi-step operations within one instruction set. It  is the design of the CPU where one instruction performs many low-level operations. For example,  memory storage, an  arithmetic operation and loading from memory. The CISC approach attempts to minimize the number of instructions per program, sacrificing the number of cycles per instruction. Computers based on the CISC architecture are designed to decrease the memory cost. Because, the large programs need more storage, thus increasing the memory cost and large memory becomes more expensive. To solve these problems, the number of instructions per program can be reduced by embedding the number of operations in a single instruction, thereby making the instructions more complex.



#### Examples of CISC PROCESSORS

****IBM 370/168**** – It was introduced in the year 1970. CISC design is a 32 bit processor and four 64-bit floating point registers.  
****VAX 11/780**** – CISC design is a 32-bit processor and it supports many numbers of addressing modes and machine instructions which is from Digital Equipment Corporation.  
****Intel 80486**** – It was launched in the year 1989 and it is a CISC processor, which has instructions varying lengths from 1 to 11 and it will have 235 instructions.

#### CHARACTERISTICS OF CISC ARCHITECTURE

* Instruction-decoding logic will be Complex.
* One instruction is required to support multiple addressing modes.
* Less chip space is enough for general purpose registers for the instructions that are 0operated directly on memory.
* Various CISC designs are set up two special registers for the stack pointer, handling interrupts,  etc.
* MUL is referred to as a “complex instruction” and requires the programmer for storing functions.

1. VLIW: Very long instruction word (VLIW) describes a computer processing architecture in which a language [compiler](https://whatis.techtarget.com/definition/compiler) or pre-processor breaks program [instruction](https://whatis.techtarget.com/definition/instruction) down into basic operations that can be performed by the [processor](https://whatis.techtarget.com/definition/processor) in [parallel](https://whatis.techtarget.com/definition/parallel) (that is, at the same time). These operations are put into a very long instruction [word](https://whatis.techtarget.com/definition/word) which the processor can then take apart without further analysis, handing each operation to an appropriate functional unit. VLIW is sometimes viewed as the next step beyond the reduced instruction set computing ( [RISC](https://search400.techtarget.com/definition/RISC) ) architecture, which also works with a limited set of relatively basic instructions and can usually execute more than one instruction at a time (a characteristic referred to as superscalar ). The main advantage of VLIW processors is that complexity is moved from the hardware to the software, which means that the hardware can be smaller, cheaper, and require less power to operate. The challenge is to design a compiler or pre-processor that is intelligent enough to decide how to build the very long instruction words. If dynamic pre-processing is done as the program is run, performance may be a concern. An example of a processor that uses the VLIW architecture is the crusoe family of processors from Transmeta.

