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Course: CSC 310

Department: Computer Science

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1) RISC (2) CISC (3) VLIW

1) RISC architecture - (Reduced Instruction Set Computer): is a CPU design strategy based on the insight that simplified instruction set gives higher Pegormance when combined with a microprocessor architecture which, has the abuity to execute by using some microprocessor cycles per instruction (watelectronics, 2019)

2) CISC ~~bare~~ ~~th~~tecture (complese instruction set computer): has the abuity to execute addressing modes or multiple step operations within one instruction set. It is the design of the CPU where one instruction pegorms many low-level operation. (watelelctronics, 2019)

3) VLIW architecture (Very long instruction word) is a computer processing architecture in which a language compiler or pre-processor breaks program instructions down into basic operations that can be performed by the processor in parallel (that at the same time)