**Falola Uthman Kayode**

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**COMPUTER ENGINEERING**

Answer 1

* ASIC: Application-Specific Integrated Circuit
* PAL: Programmable Array Logic
* PLA: Programmable Logic Array
* PLD: Programmable Logic Device
* CPLD: Complex Programmable Logic Device
* FPGA: Field-Programmable Gate Array

Answer 2

Granularity of logic block has influence on performance of an FPGA. Typically higher granularity level results in lesser delay between input and output. As the granularity of logic block increases, number of levels of logic in critical path decreases, and hence delay in critical path decreases. On the flip side with increase in granularity level average fan out increases and number of switches also increases as each block has more pins. Also the length of wires increases with increase in size of logic block.

Answer 3

1. The devices typically offer a higher degree of integration as compared to discrete 7400-series or 4000-series components. They’re smaller, and use less power. In some cases, they’re re-programmable, allowing upgrades without changing the PCB.By the time you get to FPGAs, you could have a truly massive amount of reprogrammable logic. It’s simply infeasible to build that much logic in discrete components. And if you want to build a custom hardwired ASIC instead, you could be on the hook for millions.
2. Yes, many.

In the embedded world where electronics are being controlled there are many places wher a hard wired solution is the only way to go as there is a critical timing constraint. Working on a motor controller where the current in the coils has to be measured controlled, real time, in nanoseconds whilst other measurements and algorithms are being calculated. This is easy to do in hardwire, but impossible to do with current chips in software. Short of very expensive CPUs that would still have difficulty in achieving the timing constraints, a hard wired solution is the only answer.

Some of the embedded processors available today have ability to ‘hardwire’ digital, analog, and FPGA components as part of their offering. You end up with hard wired logic and function that is defined by software within a single chip.The ‘hard wiring’ is reconfigurable in development but can be locked in production. This is sometimes done by a configurable ‘mask’ at the end of the chip manufacturing process. The hard wiring is then truly ‘hard’ and impervious to neutron and magnetic bombardment. Such chips cannot be upgraded in the field.

Answer 4

Certainly, the stored program will be nonvolatile, but it will also be read-only. This is why fuse programmed devices are sometimes called ”OTP” (One-Time Programmable)

OTP (one time programmable) memory is a special type of non-volatile memory (NVM) that permits data to be written to memory only once. Once the memory has been programmed, it retains its value upon loss of power (i.e., is non-volatile). OTP memory is used in applications where reliable and repeatable reading of data is required.

Answer 5

