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**QUESTION**

Briefly explain each of the following architectures:

1. RISC

 2. CISC

 3. VLIW

**SOLUTION**

1) RISC: It is fully known as Reduced Instruction Set Computers. A **reduced instruction set computer**, or **RISC** is a computer instruction set that allows a computer's microprocessors to have fewer cycles per instructions (CPI) than a complex instruction set computer (CISC)

A RISC computer has a small set of simple and general instructions, rather than a large set of complex and specialized ones. The main distinguishing feature of RISC is that the instruction set is optimized for a highly regular instruction pipeline flow. Another common RISC trait is their load/store architecture in which memory is accessed through specific instructions rather than as a part of most instructions. It can be defined as a type of microprocessor architecture that utilizes a small, highly-optimized set of instructions, rather than a more specialized set of instructions often found in other types of architecture

2) CISC:  The term **CISC** stands for ''Complex Instruction Set Computer''. It is a CPU design plan based on single commands, which are skilled in executing multi-step operations. **CISC** computers have small programs. It has a huge number of compound instructions, which takes a long time to perform. The primary goal of CISC architecture is to complete a task in as few lines of assembly as possible. This is achieved by building processor hardware that is capable of understanding and executing a series of operations.

**Key points of CISC architecture**

I).Emphasis on hardware

ii) Multi-clock, complex instructions

iii) To memory: "LOAD" and "STORE" are incorporated in instructions

iv) High cycles per second

v) Small code sizes

vi) Transistors used for storing complex instructions

3) VLIW: It is known as Very long instruction word. The Very long instruction word (**VLIW**) describes a computer processing architecture in which a language compiler or pre-processor breaks program instruction down into basic operations that can be performed by the processor in parallel (that is, at the same time). VLIW refers to instruction set architectures designed to exploit instruction level parallelism (ILP). Whereas conventional central processing units (CPU, processor) mostly allow programs to specify instructions to execute in sequence only, a VLIW processor allows programs to explicitly specify instructions to execute in parallel. This design is intended to allow higher performance without the complexity inherent in some other designs.

The main advantage is the saving in hardware — the compiler now decides what can be executed in parallel, and the hardware just does it. There is no need to check for dependencies or decide on scheduling — the compiler has already resolved these issues.