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**CSC310**

**ASSIGNMENT**

1. **REDUCED INSTRUCTION SET COMPUTER (RISC)**

A reduced instruction set computer is a computer which only uses simple commands that can be divided into several instructions which achieve low-level operation within a single clock cycle, as its name propose “Reduced Instruction Set”. The RISC is a CPU design plan based on simple orders and acts fast. RISC is a microprocessor that is designed to carry out few instructions at the similar time. Based on small commands, these chips need fewer transistors, which make the transistors inexpensive to design and produce. The features of RISC include the following

1. The demand of decoding is less
2. Few data types in hardware
3. General purpose register identical
4. Uniform instruction set
5. Simple addressing nodes.
6. **COMPLEX INSTRUCTION SET COMPUTER (CISC)**

A complex instruction set computer is a computer where single instructions can perform numerous low-level operations like a load from memory, an arithmetic operation, and a memory store or are accomplished by multi-step processes or addressing modes in single instructions, as its name propose “Complex Instruction Set”. CISC is a CPU design plan based on single commands, which are skilled in executing multi-step operations.

CISC computers have small programs. It has a huge number of compound instructions, which takes a long time to perform. Here, a single set of instruction is protected in several steps; each instruction set has additional than 300 separate instructions. Maximum instructions are finished in two to ten machine cycles. In CISC, instruction pipelining is not easily implemented.

1. **VERY LONG INSTRUCTION WORD (VLIW)** Very long instruction word (VLIW) refers to instruction set architectures designed to exploit instruction level parallelism (ILP). Whereas conventional central processing units (CPU, processor) mostly allow programs to specify instructions to execute in sequence only, a VLIW processor allows programs to explicitly specify instructions to execute in parallel. This design is intended to allow higher performance without the complexity inherent in some other designs. The traditional means to improve performance in processors include dividing instructions into sub-steps so the instructions can be executed partly at the same time (termed pipelining), dispatching individual instructions to be executed independently, in different parts of the processor (superscalar architectures), and even executing instructions in an order different from the program (out-of-order execution). These methods all complicate hardware (larger circuits, higher cost and energy use) because the processor must make all of the decisions internally for these methods to work. In contrast, the VLIW method depends on the programs providing all the decisions regarding which instructions to execute simultaneously and how to resolve conflicts. As a practical matter, this means that the compiler (software used to create the final programs) becomes far more complex, but the hardware is simpler than in many other means of parallelism.