EJALONIBU OLUWABUSAYO MARY
15/ENG02/019
COE 506
Digital Design using VHDL

Assignment

1) ASIC - Application Specific Integrated Circuit
PAL - Programmable Array Logic
PLA - Programmable Logic Array
PLD - Programmable Logic Device
CPLD - Complex Programmable Logic Device
FPGA - Field - Programmable Gate Array

2) How granularity of logic block influences the performance of an FPGA:
The higher granularity level results in lesser delay between input and output. As the granularity of logic block increases, number of levels of logic in Critical path decreases, and hence delay in Critical path decreases. With increase in granularity level, average fan out increases and number of switches also increases as each block has more pins, Also the length of wires increase with increase in size of logic block.

3) Why would anyone use programmable logic devices in place of traditional "hard wired" logic? Are there any applications where hard-wired logic would do a better job than a programmable device?

→ Programmable logic devices are prefered because;

- It is accurate.
- It is cost efficient
- It offers simplicity

→ Yes, there are many places where hard wired logic could do better than a programmable device.

4) Some programmable devices are built with a 'security fuse' inside which prevents anyone from reverse-engineering a programmed chip. Stored programs will be nonvolatile but it will also be read-only. This is why the fused programmed devices are sometimes called OTP which means One Time Programmable. This is a memory and it is a special type of ~~memory~~ non-volitile memory (NVM) that permits data to be written only once

5) Using 4×8×4 PLA to implement the function;

$F_1(w,x,y,z) = wx'y'z + wx'yz' + wxy'$

$F_2(w,x,y,z) = wx'y + x'y'z$