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MATRIC N0: 17/SCI01/039

COURSE: CSC 310(COMPUTER ARCHITECTURE and ORGANISATION).

QUESTIONS

Briefly explain each of the following architectures:

1. RISC

2. CISC

3. VLIW.

SOLUTIONS

1. A **reduced instruction set computer** (**RISC)**: is a computer [instruction set](https://en.wikipedia.org/wiki/Instruction_set) that allows a computer's [microprocessor](https://en.wikipedia.org/wiki/Microprocessor) to have fewer [cycles per instruction](https://en.wikipedia.org/wiki/Cycles_per_instruction) (CPI) than a [complex instruction set computer](https://en.wikipedia.org/wiki/Complex_instruction_set_computer) (CISC). A RISC computer has a small set of simple and general instructions, rather than a large set of complex and specialized ones. The main distinguishing feature of RISC is that the instruction set is optimized for a highly regular [instruction pipeline](https://en.wikipedia.org/wiki/Instruction_pipeline) flow. Another common RISC trait is their [load/store architecture](https://en.wikipedia.org/wiki/Load/store_architecture),in which memory is accessed through specific instructions rather than as a part of most instructions.
2. A **complex instruction set computer** (**CISC**) is a computer in which single [instructions](https://en.wikipedia.org/wiki/Instruction_set_architecture) can execute several low-level operations (such as a load from [memory](https://en.wikipedia.org/wiki/Memory_(computers)), an [arithmetic](https://en.wikipedia.org/wiki/Arithmetic) [operation](https://en.wikipedia.org/wiki/Operator_(programming)), and a [memory store](https://en.wikipedia.org/wiki/Memory_(computers))) or are capable of multi-step operations or [addressing modes](https://en.wikipedia.org/wiki/Addressing_mode) within single instructions. and has therefore become something of an [umbrella term](https://en.wikipedia.org/wiki/Umbrella_term) for everything that is not RISC, from large and complex [mainframe computers](https://en.wikipedia.org/wiki/Mainframe_computer) to simplistic microcontrollers where memory load and store operations are not separated from arithmetic instructions. The only typical differentiating characteristic is that most RISC designs use uniform instruction length for almost all instructions, and employ strictly separate load/store-instructions.
3. **Very long instruction word (VLIW)**: describes a computer processing architecture in which a language [compiler](https://whatis.techtarget.com/definition/compiler) or pre-processor breaks program [instruction](https://whatis.techtarget.com/definition/instruction) down into basic operations that can be performed by the [processor](https://whatis.techtarget.com/definition/processor) in [parallel](https://whatis.techtarget.com/definition/parallel) (that is, at the same time). These operations are put into a very long instruction [word](https://whatis.techtarget.com/definition/word) which the processor can then take apart without further analysis, handing each operation to an appropriate functional unit.