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15/ENG02/031

COE 506

DIGITAL SYSTEM DESIGN USING VHDL

ASSIGNMENT

QUESTION 1

1. ASIC -Application Specific Integrated Circuits
2. PAL- Programmable Array Logic
3. PLA-Programmable Logic Array
4. PLD- Programmable Logic Device
5. CPLD- Complex Programmable Logic Device
6. FPGA- Field-Programmable Gate Array

QUESTION 2

In typical situations, higher granularity levels results in lesser delay between input and output. As the granularity of logic block increases, number of levels of logic in critical path decreases and hence delay in critical path decreases.

QUESTION 3

3a) Why would anyone use programmable logic devices in place of traditional hard-wired logic?

- Density, and its closely related cousin,
- Cost.

The “traditional” gates that you might find in a 74xx series chip require that you have quite a few of them in order to perform relatively simple combinational logic functions, whereas programmable logic gets you equivalent or better capability in a much smaller space, which consumes less board area, which reduces the cost and size of the board. Furthermore, the programmable logic costs less $ per gate, and increasingly so as you move to higher capacities such as in the highly efficient CPLDs and FPGAs. The designs you can fit in a single FPGA can, and do, replace entire boards of “traditional logic” gates, CPUs, memories, and all, when used to retrofit older equipment. If you make a design error, you just reprogram the device to fix the bug rather than re-wiring or redesigning the circuit board

- In general, its faster and cleaner and easier to modify and upgrade. And physically smaller and more easily configurable.

3b) Are there any applications where hard-wired logic would be a better job than a programmable device?

Yes, many.

In the embedded world where electronics are being controlled there are many places where a hard wired solution is the only way to go as there is a critical timing constraint. Short of very expensive CPUs that would still have difficulty in achieving the timing constraints, a hard wired solution is the only answer. Some of the embedded processors available today have ability to ‘hardwire’ digital, analog, and FPGA components as part of their offering. You end up with hard wired logic and function that is defined by software within a single chip.

The ‘hard wiring’ is reconfigurable in development but can be locked in production. This is sometimes done by a configurable ‘mask’ at the end of the chip manufacturing process. The hard wiring is then truly ‘hard’ and impervious to neutron and magnetic bombardment. Such chips cannot be upgraded in the field. Also when cost is a factor, programmable IC’s cost more than discrete logic and require extra design tools. HW circuits don't need programing. Unless the circuit is extensive, discrete logic is lower cost and faster to produce.

QUESTION 4

The stored program will definitely be non-volatile but it will also be read-only. This is why fused-programmed devices are also called OTP (One time programmable). It is also interesting to know that some programmable devices are built with a security fuse inside which prevents anyone from reverse-engineering programmed chip.

QUESTION 5

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5.)

$f_1(w\,x\,y\,z) = w\bar{x}\bar{y}z + w\bar{x}y\bar{z} + wx\bar{y}$

$f_2(w\,x\,y\,z) = w\bar{x}y + \bar{x}\bar{y}z$

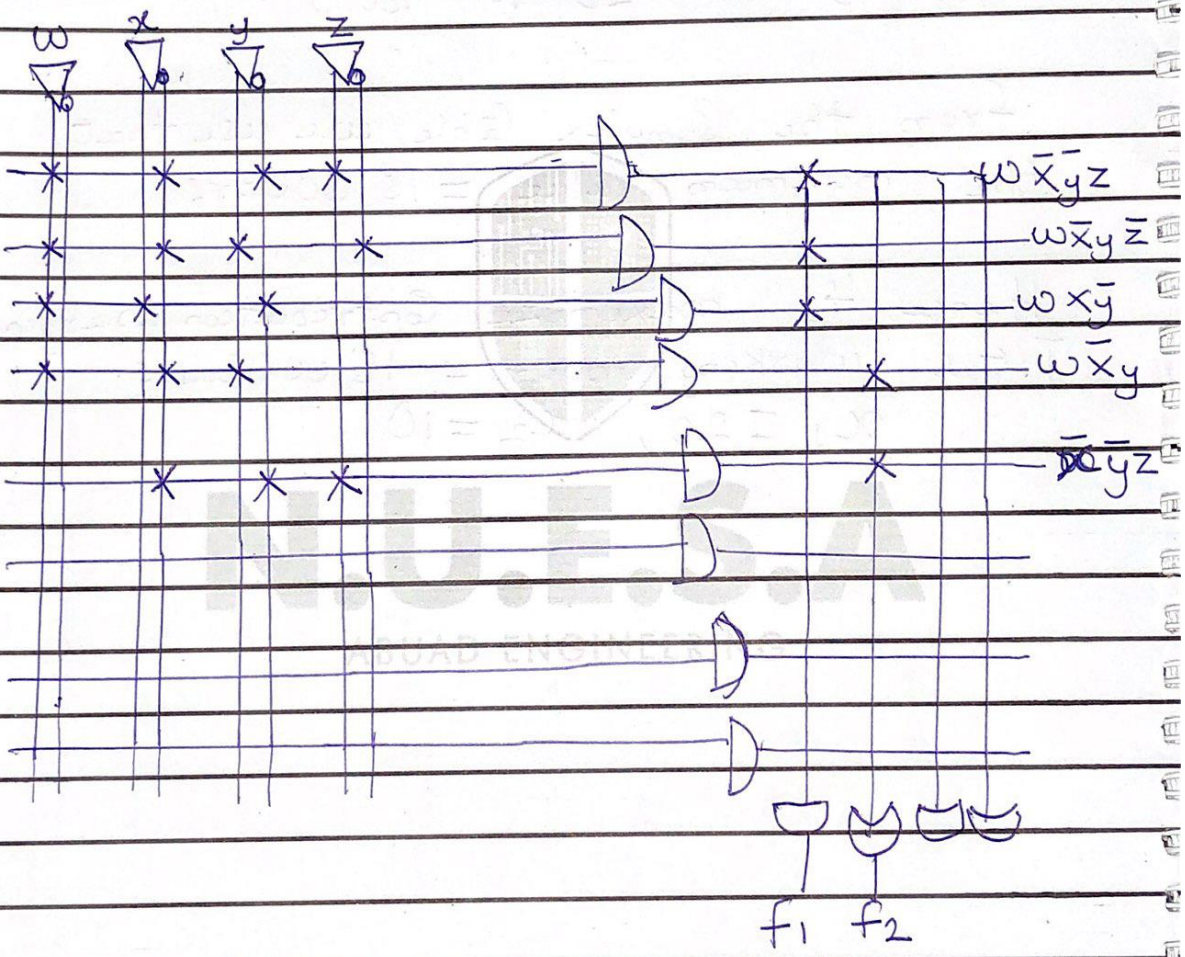

figure: 4x8x4 PLA implementation of the function.