**COLE EMMANUEL ROTIMI**

**15/ENG02/016**

**COMPUTER ENGINEERING**

**COE 506**

**DIGITL DESIGN USING VDHL**

**QUESTION 1**

**ASIC**:

 An **application-specific integrated circuit** is an [integrated circuit](https://en.wikipedia.org/wiki/Integrated_circuit%22%20%5Co%20%22Integrated%20circuit) (IC) chip customized for a particular use, rather than intended for general-purpose use. For example, a chip designed to run in a [digital voice recorder](https://en.wikipedia.org/wiki/Digital_voice_recorder%22%20%5Co%20%22Digital%20voice%20recorder). [Application-specific standard product](https://en.wikipedia.org/wiki/Application-specific_integrated_circuit%22%20%5Cl%20%22Application-specific_standard_product) (ASSP) chips are intermediate between ASIC and industry standard integrated circuits like the [7400 series](https://en.wikipedia.org/wiki/7400_series%22%20%5Co%20%227400%20series) or the [4000 series](https://en.wikipedia.org/wiki/4000_series%22%20%5Co%20%224000%20series).

ASIC chips are typically [fabricated](https://en.wikipedia.org/wiki/Semiconductor_device_fabrication%22%20%5Co%20%22Semiconductor%20device%20fabrication) using [metal-oxide-semiconductor](https://en.wikipedia.org/wiki/Metal-oxide-semiconductor%22%20%5Co%20%22Metal-oxide-semiconductor) (MOS) technology, as [MOS integrated circuit](https://en.wikipedia.org/wiki/MOS_integrated_circuit%22%20%5Co%20%22MOS%20integrated%20circuit) chips.

**PAL**:

**Programmable Array Logic** (**PAL**) is a family of [programmable logic device](https://en.wikipedia.org/wiki/Programmable_logic_device%22%20%5Co%20%22Programmable%20logic%20device) semiconductors used to implement [logic](https://en.wikipedia.org/wiki/Logic%22%20%5Co%20%22Logic) functions in digital [circuits](https://en.wikipedia.org/wiki/Electrical_network%22%20%5Co%20%22Electrical%20network) introduced by [Monolithic Memories](https://en.wikipedia.org/wiki/Monolithic_Memories%22%20%5Co%20%22Monolithic%20Memories), Inc. (MMI) in March 1978. MMI obtained a registered trademark on the term PAL for use in "Programmable Semiconductor Logic Circuits". The trademark is currently held by [Lattice Semiconductor](https://en.wikipedia.org/wiki/Lattice_Semiconductor%22%20%5Co%20%22Lattice%20Semiconductor).

**PLA**:

A **programmable logic array** (**PLA**) is a kind of [programmable logic device](https://en.wikipedia.org/wiki/Programmable_logic_device%22%20%5Co%20%22Programmable%20logic%20device) used to implement [combinational logic](https://en.wikipedia.org/wiki/Combinational_logic%22%20%5Co%20%22Combinational%20logic) [circuits](https://en.wikipedia.org/wiki/Electrical_network%22%20%5Co%20%22Electrical%20network). The PLA has a set of programmable [AND gate](https://en.wikipedia.org/wiki/AND_gate%22%20%5Co%20%22AND%20gate) planes, which link to a set of programmable [OR gate](https://en.wikipedia.org/wiki/OR_gate%22%20%5Co%20%22OR%20gate) planes, which can then be conditionally complemented to produce an output. It has 2N AND Gates for N input variables, and for M outputs from PLA, there should be M OR Gates, each with programmable inputs from all of the AND gates. This layout allows for many logic functions to be synthesized in the sum of products [canonical forms](https://en.wikipedia.org/wiki/Canonical_form_%28Boolean_algebra%29%22%20%5Co%20%22Canonical%20form%20%28Boolean%20algebra%29).

**PLD**:

A **programmable logic device** (**PLD**) is an [electronic](https://en.wikipedia.org/wiki/Electronics%22%20%5Co%20%22Electronics) component used to build [reconfigurable](https://en.wikipedia.org/wiki/Reconfigurable_computing%22%20%5Co%20%22Reconfigurable%20computing) [digital circuits](https://en.wikipedia.org/wiki/Digital_electronics%22%20%5Co%20%22Digital%20electronics). Unlike [integrated circuits](https://en.wikipedia.org/wiki/Integrated_circuit%22%20%5Co%20%22Integrated%20circuit) (IC) which consist of [logic gates](https://en.wikipedia.org/wiki/Logic_gate%22%20%5Co%20%22Logic%20gate) and have a fixed function, a PLD has an undefined function at the [time of manufacture](https://en.wikipedia.org/wiki/Tape-out%22%20%5Co%20%22Tape-out). Before the PLD can be used in a circuit it must be programmed (reconfigured) by using a specialized program

**CPLD**:

A **complex programmable logic device** (**CPLD**) is a [programmable logic device](https://en.wikipedia.org/wiki/Programmable_logic_device%22%20%5Co%20%22Programmable%20logic%20device) with complexity between that of [PALs](https://en.wikipedia.org/wiki/Programmable_Array_Logic%22%20%5Co%20%22Programmable%20Array%20Logic) and [FPGAs](https://en.wikipedia.org/wiki/Field-programmable_gate_array%22%20%5Co%20%22Field-programmable%20gate%20array), and architectural features of both. The main building block of the CPLD is a [macrocell](https://en.wikipedia.org/wiki/Macrocell_array%22%20%5Co%20%22Macrocell%20array), which contains logic implementing [disjunctive normal form](https://en.wikipedia.org/wiki/Disjunctive_normal_form%22%20%5Co%20%22Disjunctive%20normal%20form) expressions and more specialized logic operations

**FPGA**:

A **field-programmable gate array** (**FPGA**) is an [integrated circuit](https://en.wikipedia.org/wiki/Integrated_circuit%22%20%5Co%20%22Integrated%20circuit) designed to be configured by a customer or a designer after manufacturing – hence the term "[field-programmable](https://en.wikipedia.org/wiki/Field-programmability%22%20%5Co%20%22Field-programmability)". The FPGA configuration is generally specified using a [hardware description language](https://en.wikipedia.org/wiki/Hardware_description_language%22%20%5Co%20%22Hardware%20description%20language) (HDL), similar to that used for an [application-specific integrated circuit](https://en.wikipedia.org/wiki/Application-Specific_Integrated_Circuit%22%20%5Co%20%22Application-Specific%20Integrated%20Circuit) (ASIC). [Circuit diagrams](https://en.wikipedia.org/wiki/Circuit_diagram%22%20%5Co%20%22Circuit%20diagram) were previously used to specify the configuration, but this is increasingly rare due to the advent of [electronic design automation](https://en.wikipedia.org/wiki/Electronic_design_automation%22%20%5Co%20%22Electronic%20design%20automation) tools.

FPGAs contain an array of [programmable](https://en.wikipedia.org/wiki/Programmable_logic_device%22%20%5Co%20%22Programmable%20logic%20device) [logic blocks](https://en.wikipedia.org/wiki/Logic_block%22%20%5Co%20%22Logic%20block), and a hierarchy of "reconfigurable interconnects" that allow the blocks to be "wired together", like many logic gates that can be inter-wired in different configurations. [Logic blocks](https://en.wikipedia.org/wiki/Logic_block%22%20%5Co%20%22Logic%20block) can be configured to perform complex [combinational functions](https://en.wikipedia.org/wiki/Combinational_logic%22%20%5Co%20%22Combinational%20logic), or merely simple [logic gates](https://en.wikipedia.org/wiki/Logic_gate%22%20%5Co%20%22Logic%20gate) like [AND](https://en.wikipedia.org/wiki/AND_gate%22%20%5Co%20%22AND%20gate) and [XOR](https://en.wikipedia.org/wiki/XOR_gate%22%20%5Co%20%22XOR%20gate). In most FPGAs, logic blocks also include [memory elements](https://en.wikipedia.org/wiki/Memory_cell_%28computing%29%22%20%5Co%20%22Memory%20cell%20%28computing%29), which may be simple [flip-flops](https://en.wikipedia.org/wiki/Flip-flop_%28electronics%29%22%20%5Co%20%22Flip-flop%20%28electronics%29) or more complete blocks of memory. Many FPGAs can be reprogrammed to implement different [logic functions](https://en.wikipedia.org/wiki/Boolean_function%22%20%5Co%20%22Boolean%20function),  allowing flexible [reconfigurable computing](https://en.wikipedia.org/wiki/Reconfigurable_computing%22%20%5Co%20%22Reconfigurable%20computing) as performed in [computer software](https://en.wikipedia.org/wiki/Software%22%20%5Co%20%22Software).

**QUESTION 2**

**Granularity of logic block** has **influence** on **performance of an FPGA**. Typically higher **granularity** level results in lesser delay between input and output. As the **granularity of logic block** increases, number of levels of **logic** in critical path decreases, and hence delay in critical path decreases.

 On the flip side with increase in granularity level average fan out increases and number of switches also increases as each block has more pins. Also the length of wires increases with increase in size of logic block.

**QUESTION 3**

Programmable logic devices which can be reprogrammed or reconfigured to perform specific functions. Unlike devices which perform fixed functions assigned to them at the point of manufacturing, programmable devices use logic.This allows flexibility in their operations through reconfiguration.

Compared to a ****logic**** gate, which has a fixed function, a PLD has an undefined function at the time of manufacture. Before the PLD can be used in a circuit it must be ****programmed****, that is, reconfigured.The configuration of the internal logic is done by the user.

****A logic device**** is a small semi conductors that process digital data in order to control the operations of an electronic system.

PLD Store permanent binary information (nonvolatile) which can be read only (cannot be altered). Information is specified by designer and physically inserted (embedded) into the PLD.

****Why make devices programmable****

Reduce total cost as the design is faster and requires minimal time.

Flexible: They allow last minute changes often without having to redesign the circuit board. This reduces the risk associated with the production.

Making devices programmable can also allows improvements in the devices even without improvements in the hardware. For a device to be programmable, it has to have certain features:

Processor, Memory unit, Power supply, I/O modules, Programming device

With these components, one can easily program a device and thus the rise of programmable logic devices.

ADVANTAGES OF HARD WIRED

 They operate at very high speeds making it crucial for real time and other applications where time is a major factor. Hardwired control units don’t need separate control memory for storage of control word for generation of control signals. They perform the same task using logical circuitry which is also the reason they are so fast. Hardwired control units are known to be more power efficient than their counterparts making them an ideal choice for processors in mobile devices. Hardwired control units are now widely employed in RISC processors which are known for their speed, reduced instruction set and support for limited addressing modes

**QUESTION 4**

Some programmable devices (Texas Instruments’ TIBPAL series, for example) are built with a ”security fuse” inside which prevents anyone from reverse-engineering a programmed chip

**QUESTION 5**

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