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Assignment:

* Risc (reduced instruction set computer): RISC, or *Reduced Instruction Set Computer*. is a type of microprocessor architecture that utilizes a small, highly-optimized set of instructions, rather than a more specialized set of instructions often found in other types of architectures. The main distinguishing feature of RISC is that the instruction set is optimized for a highly regular [instruction pipeline](https://en.wikipedia.org/wiki/Instruction_pipeline) flow. Characteristics- Most RISC architectures have fixed-length instructions (commonly 32 bits) and a simple encoding, which simplifies fetch, decode, and issue logic considerably. For any given level of general performance, a RISC chip will typically have far fewer [transistors](https://en.wikipedia.org/wiki/Transistor) dedicated to the core logic which originally allowed designers to increase the size of the register set and increase internal parallelism. Simple Instructions are used in RISC architecture.
* RISC helps and supports few simple data types and synthesize complex data types.
* RISC utilizes simple addressing modes and fixed length instructions for pipelining.
* RISC permits any register to use in any context.
* One Cycle Execution Time
* The amount of work that a computer can perform is reduced by separating “LOAD” and “STORE” instructions.
* RISC contains Large Number of Registers in order to prevent various number of interactions with memory.

Advantages

* RISC([Reduced instruction set computing](http://en.wikipedia.org/wiki/Reduced_instruction_set_computing))architecture has a set of instructions, so high-level language compilers can produce more efficient code
* It allows freedom of using the space on microprocessors because of its simplicity.
* Many RISC processors use the registers for passing arguments and holding the local variables.
* RISC functions use only a few parameters, and the RISC processors cannot use the call instructions, and therefore, use a fixed length instruction which is easy to pipeline.
* The speed of the operation can be maximized and the execution time can be minimized.

Disadvantages

* Mostly, the performance of the RISC processors depends on the programmer or compiler as the knowledge of the compiler plays a vital role while changing the CISC code to a RISC code
* While rearranging the CISC code to a RISC code, termed as a code expansion, will increase the size. And, the quality of this code expansion will again depend on the compiler, and also on the machine’s instruction set.
* The first level cache of the RISC processors is also a disadvantage of the RISC, in which these processors have large memory caches on the chip itself. For feeding the instructions, they require very fast memory systems.

Cisc (complex instruction set computer): the CISC approach attempts to minimize the number of instructions per program, sacrificing the number of cycles per instruction. Computers based on the CISC architecture are designed to decrease the memory cost. Because, the large programs need more storage, thus increasing the memory cost and large memory becomes more expensive. To solve these problems, the number of instructions per program can be reduced by embedding the number of operations in a single instruction, thereby making the instructions more complex.

Examples of cisc-**IBM 370/168** – It was introduced in the year 1970. CISC design is a 32 bit processor and four 64-bit floating point registers.
**VAX 11/780** – CISC design is a 32-bit processor and it supports many numbers of addressing modes and machine instructions which is from Digital Equipment Corporation.
**Intel 80486** – It was launched in the year 1989 and it is a CISC processor, which has instructions varying lengths from 1 to 11 and it will have 235 instructions.

Characteristics of cisc

* Instruction-decoding logic will be Complex.
* One instruction is required to support multiple addressing modes.
* Less chip space is enough for general purpose registers for the instructions that are 0operated directly on memory.
* Various CISC designs are set up two special registers for the stack pointer, handling interrupts,  etc.
* MUL is referred to as a “complex instruction” and requires the programmer for storing functions.

Advantages

* Microprogramming is easy assembly language to implement, and less expensive than hard wiring a control unit.
* The ease of microcoding new instructions allowed designers to make CISC machines upwardly compatible:
* As each instruction became more accomplished, fewer instructions could be used to implement a given task.

**Disadvantages of CISC architecture**

* The performance of the machine slows down due to the amount of clock time taken by different instructions will be dissimilar
* Only 20% of the existing instructions is used in a typical programming event, even though there are various specialized instructions in reality which are not even used frequently.
* The conditional codes are set by the CISC instructions as a side effect of each instruction which takes time for this setting – and, as the subsequent instruction changes the condition code bits – so, the compiler has to examine the condition code bits before this happens.

Vliw (very long instruction word) architecture: Very long instruction word (VLIW) refers to [instruction set architectures](https://en.wikipedia.org/wiki/Instruction_set_architecture) designed to exploit [instruction level parallelism](https://en.wikipedia.org/wiki/Instruction_level_parallelism) (ILP). Very long instruction word (VLIW) describes a computer processing architecture in which a language [compiler](https://whatis.techtarget.com/definition/compiler) or pre-processor breaks program [instruction](https://whatis.techtarget.com/definition/instruction) down into basic operations that can be performed by the [processor](https://whatis.techtarget.com/definition/processor) in [parallel](https://whatis.techtarget.com/definition/parallel) (that is, at the same time). These operations are put into a very long instruction [word](https://whatis.techtarget.com/definition/word) which the processor can then take apart without further analysis, handing each operation to an appropriate functional unit.