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**CSC 310**

1. **RISC:**

RISC, or *Reduced Instruction Set Computer*. is a type of microprocessor architecture that utilizes a small, highly-optimized set of instructions, rather than a more specialized set of instructions often found in other types of architectures. It is a [microprocessor](https://whatis.techtarget.com/definition/microprocessor-logic-chip) that is designed to perform a smaller number of types of computer [instruction](https://whatis.techtarget.com/definition/instruction)s so that it can operate at a higher speed (perform more millions of instructions per second, or [MIPS](https://searchitoperations.techtarget.com/definition/MIPS-million-instructions-per-second)). Since each instruction type that a computer must perform requires additional transistors and circuitry, a larger list or set of computer instructions tends to make the microprocessor more complicated and slower in operation. The RISC concept has led to a more thoughtful design of the microprocessor. Among design considerations are how well an instruction can be mapped to the clock speed of the microprocessor (ideally, an instruction can be performed in one clock cycle); how "simple" an architecture is required; and how much work can be done by the microchip itself without resorting to software help.

1. **CISC:**

Stands for "Complex Instruction Set Computing." This is a type of microprocessor design. The CISC architecture contains a large set of computer instructions that range from very simple to very complex and specialized. Though the design was intended to compute complex instructions in the most efficient way, it was later found that many small, short instructions could compute complex instructions more efficiently. This led to a design called Reduced Instruction Set Computing (RISC), which is now the other major kind of microprocessor architecture. CISC has the ability to execute addressing modes or multi-step operations within one instruction set. It  is the design of the CPU where one instruction performs many low-level operations. For example,  memory storage, an  arithmetic operation and loading from memory. The CISC approach attempts to minimize the number of instructions per program, sacrificing the number of cycles per instruction. Computers based on the CISC architecture are designed to decrease the memory cost. Because, the large programs need more storage, thus increasing the memory cost and large memory becomes more expensive. To solve these problems, the number of instructions per program can be reduced by embedding the number of operations in a single instruction, thereby making the instructions more complex.

1. **VLIW:**

Very long instruction word (VLIW) describes a computer processing architecture in which a language [compiler](https://whatis.techtarget.com/definition/compiler) or pre-processor breaks program [instruction](https://whatis.techtarget.com/definition/instruction) down into basic operations that can be performed by the [processor](https://whatis.techtarget.com/definition/processor) in [parallel](https://whatis.techtarget.com/definition/parallel) (that is, at the same time). These operations are put into a very long instruction [word](https://whatis.techtarget.com/definition/word) which the processor can then take apart without further analysis, handing each operation to an appropriate functional unit. VLIW is sometimes viewed as the next step beyond the reduced instruction set computing ( [RISC](https://search400.techtarget.com/definition/RISC) ) architecture, which also works with a limited set of relatively basic instructions and can usually execute more than one instruction at a time (a characteristic referred to as *superscalar* ). The main advantage of VLIW processors is that complexity is moved from the hardware to the software, which means that the hardware can be smaller, cheaper, and require less power to operate. The challenge is to design a compiler or pre-processor that is intelligent enough to decide how to build the very long instruction words. If dynamic pre-processing is done as the program is run, performance may be a concern.