NAME: OFILI NGOZICHUKWUKA TAMARALAYEFA

MATRIC NO: **17/SCI01/061**

COURSE CODE: **CSC 310**

**ASSIGNMENT**

Briefly explain each of the following architectures:

1. RISC

2. CISC

3. VLIW.

**ANSWER**

1. **REDUCED INSTRUCTION SET COMPUTER(RISC)**: RISC is a type of microprocessor architecture that utilizes a small, highly-optimized set of instructions, rather than a more specialized set of instructions often found in other types of architectures. RISC is used in portable devices due to its power efficiency. For Example, Apple iPod and Nintendo DS. RISC does the opposite, reducing the cycles per instruction at the cost of the number of instructions per program Pipelining is one of the unique feature of RISC. It is performed by overlapping the execution of several instructions in a pipeline fashion. It has a high performance advantage over CISC. RISC processors take simple instructions and are executed within a clock cycle.

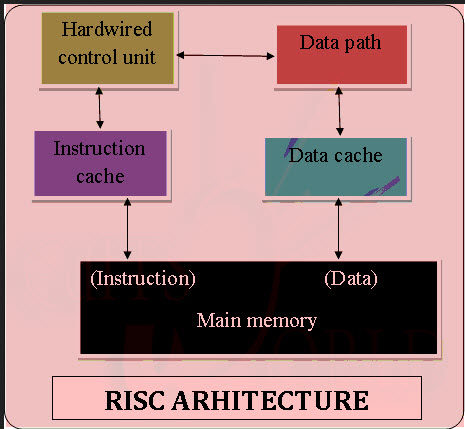
****

Figure1: RISC Architecture

1. **COMPLEX INSTRUCTION SET COMPUTING(CISC):** The CISC architecture contains a large set of computer instructions that range from very simple to very complex and specialized. Though the design was intended to compute complex instructions in the most efficient way, it was later found that many small, short instructions could compute complex instructions more efficiently. This led to a design called Reduced Instruction Set Computing (RISC), which is now the other major kind of microprocessor architecture. Intel Pentium processors are mainly CISC-based, with some RISC facilities built into them, whereas the PowerPC processors are completely RISC-based. The CISC approach attempts to minimize the number of instructions per program, sacrificing the number of cycles per instruction. Computers based on the CISC architecture are designed to decrease the memory cost. Because, the large programs need more storage, thus increasing the memory cost and large memory becomes more expensive. To solve these problems, the number of instructions per program can be reduced by embedding the number of operations in a single instruction, thereby making the instructions more complex.

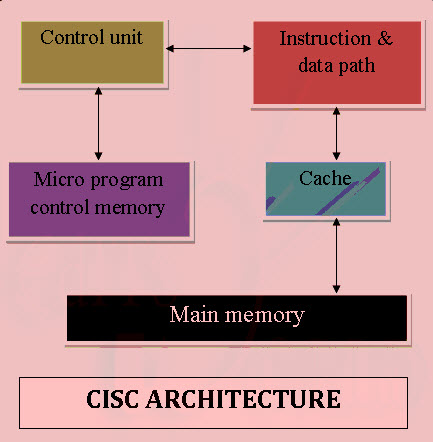


Figure2: CISC Architecture

1. **VERY LONG INSTRUCTION WORD (VLIW):** VLIW describes a computer processing architecture in which a language [compiler](https://whatis.techtarget.com/definition/compiler) or pre-processor breaks program [instruction](https://whatis.techtarget.com/definition/instruction) down into basic operations that can be performed by the [processor](https://whatis.techtarget.com/definition/processor) in [parallel](https://whatis.techtarget.com/definition/parallel) (that is, at the same time). These operations are put into a very long instruction [word](https://whatis.techtarget.com/definition/word) which the processor can then take apart without further analysis, handing each operation to an appropriate functional unit. VLIW is sometimes viewed as the next step beyond the reduced instruction set computing ( [RISC](https://search400.techtarget.com/definition/RISC) ) architecture, which also works with a limited set of relatively basic instructions and can usually execute more than one instruction at a time (a characteristic referred to as *superscalar* ). The main advantage of VLIW processors is that complexity is moved from the hardware to the software, which means that the hardware can be smaller, cheaper, and require less power to operate. The challenge is to design a compiler or pre-processor that is intelligent enough to decide how to build the very long instruction words. If dynamic pre-processing is done as the program is run, performance may be a concern.

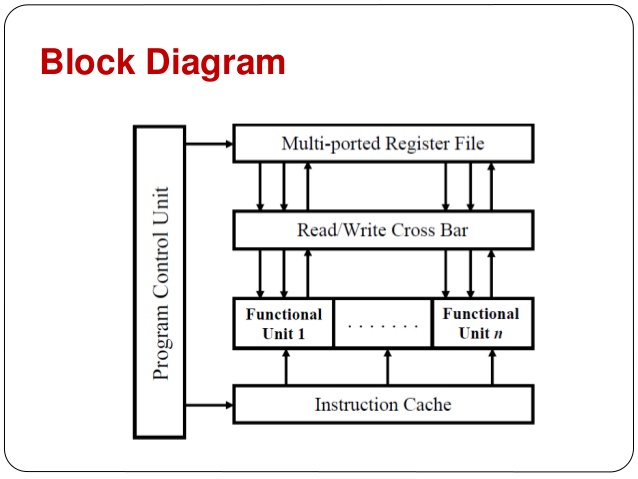


Figure3: VLIW Architecture