MANASSEH DAVID
15/ENG02/036

ASIC: → Application-Specific Integrated Circuit is a microchip designed for special application. Such as a particular kind of transmission protocol.

PAL → Programmable Array Logic: They provide only a single level of programmability, consisting of a programmable wired AND plane that feeds fixed OR-gates.

PLA → Programmable logic device Array: is a circuit that allows implementing Boolean functions in form of product form.

CPLD → Complex Programmable Logic Devices: They can be thought as multiple PLD's in a single chip. The larger size of a CPLD allows to implement either more logic equations or more complicated design.

FPGA: Field programmable Gate Array: Is an integrated circuit that can be customized for specific application. It can be configured by the user after manufacturing.

PLD: Programmable logic device:

(2) Higher granularity level results in lesser delay between the input & output. As granularity of logic blocks increases, number of levels of logic in critical path decreases, so delay in the path decreases.

3)

They could use programmable logic devices because they're smaller & use less power. In some cases, they're reprogrammable, allowing upgrades without changing the PCB.
And yes, they're cases where hard wired logic would do a better job because of critical timing constraints. Working on a motor controller where the current in the coil has to be measured, controlled, real time, in nanoseconds whilst other measurements & algorithms are being calculated. It's easier done with hard wire.

4. The stored program will be non-volatile, but it'll also be read-only. This is why fuse programmed devices are sometimes called OTP.

5) $F_1(w, x, y, z) = w\bar{x}\bar{y}z + w\bar{x}y\bar{z} + wx\bar{y}$

$F_2(w, x, y, z) = w\bar{x}y + \bar{x}\bar{y}z$