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**COMPUTER ENGINEERING**

**COE506 ASSIGNMENT**

**QUESTION 1**

* ASIC – Application Specific Integrated Circuits
* PAL – Programmable Array Logic
* PLA – Programmable Logic Array
* PLD – Programmable Logic Device
* CPLD – Complex Programmable Logic Device
* FPGA – Field Programmable Gate Array

**ASIC – Application Specific Integrated Circuits**; is a way to design integrated circuits to meet a specific application instead of using a programmable circuit. One example of this would be the 555 timer IC circuit.

**PAL – Programmable Array Logic**; In a PAL an AND plane is created to program the connectivity between the inputs and outputs of various logic circuits to produce a chip that can be programmed to supply many different logic configurations.

**PLA – Programmable Logic Array;** is a kind of programmable logic device used to implement combinationallogiccircuits. The PLA has a set of programmable AND gate planes, which link to a set of programmable OR gate planes, which can then be conditionally complemented to produce an output.

**PLD – Programmable Logic Device;** a generic term for an [integrated circuit](https://www.webopedia.com/TERM/I/integrated_circuit_IC.html) that can be programmed in a laboratory to perform complex functions. A PLD consists of arrays of AND and OR gates. A system designer implements a logic design with a device programmer that blows fuses on the PLD to control gate operation.

**CPLD – Complex Programmable Logic Device;** it is a one[kind of integrated circuit](https://www.elprocus.com/how-integrated-circuits-work-physically/) that application designers design to implement digital hardware like mobile phones.

**FPGA – Field Programmable Gate Array;** is an integrated **circuit** that can be customized for a specific application. Unlike traditional CPUs, FGPAs are "field-programmable," meaning they can be configured by the user after manufacturing.

**QUESTION 2**

The granularity of logic block has an influence on the performance of an FPGA. Typically, a higher granularity level results in a shorter delay. As the granularity of logic block increases, the number of levels of logic in critical path decreases, and hence delay in critical path decreases. However, with an increase in the granularity level; the average fan out increases as does the number of switches as each block now has more pins. Also, the length of wires increases with the increase in the size of the logic block.

**QUESTION 3**

There are a few reasons to use programmable devices instead of hard-wired logic, some are stated below;

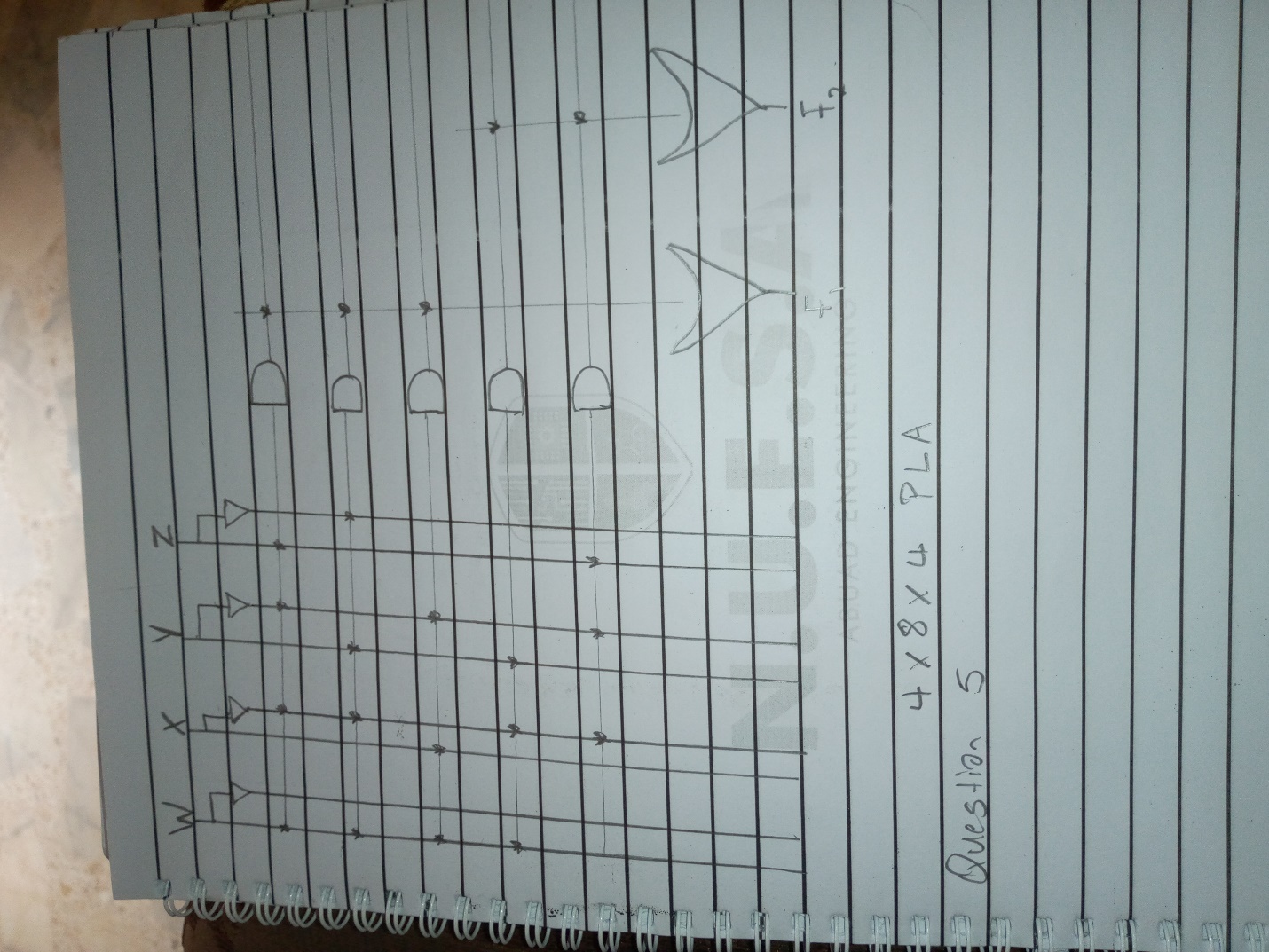
1. Fewer parts, instead of a large number of parts.
2. A PCB design can be fixed for the known inputs and outputs once defined, before the entire working logic schematic is known. Thus hardware and logic design can be carried on in parallel rather than in sequence which takes longer development time
3. As long as the I/Os are connected right, the PCB can be used for development while making changes in code on PCs and not having to make hardware cuts and jumps to fix problems as they are found.
4. Easy to add field modifications by loading new code to the in-circuit programmable device or replacing a chip in a socket.
5. Troubleshooting the problems with solder joints and trace failures plus the amount of PCB space which these low level parts occupy and layout problems is a lose lose situation.
6. They hide the circuit, they can be fixed by changing the program code, they occupy a LOT less PCB space, they are much more reliable and require negligible production trouble shooting time, Products made with old hard wired technology are simply not competitive.

In general, its faster and cleaner and easier to modify and upgrade. And physically smaller and more easily configurable.

**QUESTION 4**

Certainly, the stored program will be nonvolatile, but it will also be read-only. This is why these devices are therefore sometimes ‘one time programmable’ (OTP) and cannot be reprogrammed.

**QUESTION 5**

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