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ISIENG02/025
COMPUTER ENGINEERING VHDL ASSIGNMENT

Q1
- PAL - Programmable Array Logic
- PLA - Programmable Logic Array
- PLD - Programmable Logic Device
- ASIC - Application Specific Integrated Circuits
- FPGA - Field Programmable Gate Array
- CPLD -

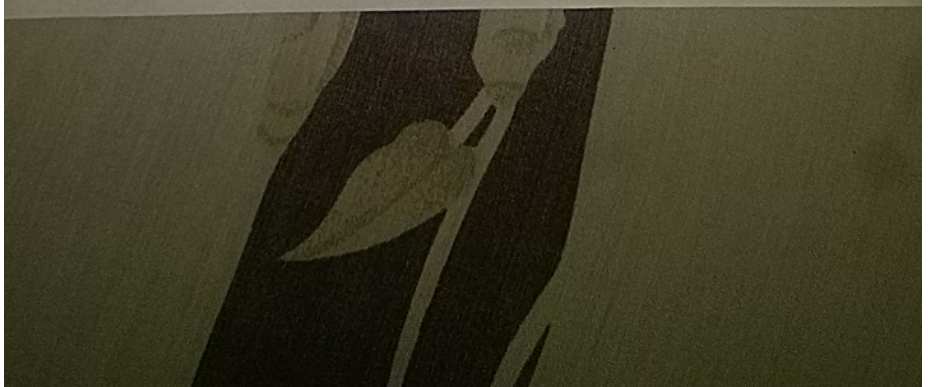
Q2
The granularity of the logic block has a significant effect on the performance of the FPGA. Typically higher granularity level results in lesser delay between input and output. As the granularity of the logic block increases, the number of levels of logic in the critical path decreases, hence delay in critical path decreases

Q3
i) It is faster to troubleshoot the faulty components.
ii) The amount of wires can be reduced by PLD
iii) Easier to manipulate the input and output logic control.

Are there any applications where hard-wired logic would be better do a bether job than a programmable device?

i) For a very high speed requirement such as turbomachinery over speed protection (gas turbines), a programmable system may also not be advisable design choice due to the speed of the response required.

ii) For systems that lacks software cie it is more straightforward to use hard wired logic.



Q4 The stored programm will be nonvolatile and read-only. This is why fuse program devices are sometimes called otp which is an acronym for "one time programmable". The memory is a special type of non-volatile memory (NVM) that permits data to be written to memory only once, once it has been programmed (i.e the memory, it retains the values upon loss of power. OTP is used in applications where reliable and repeatable reading of data is required.

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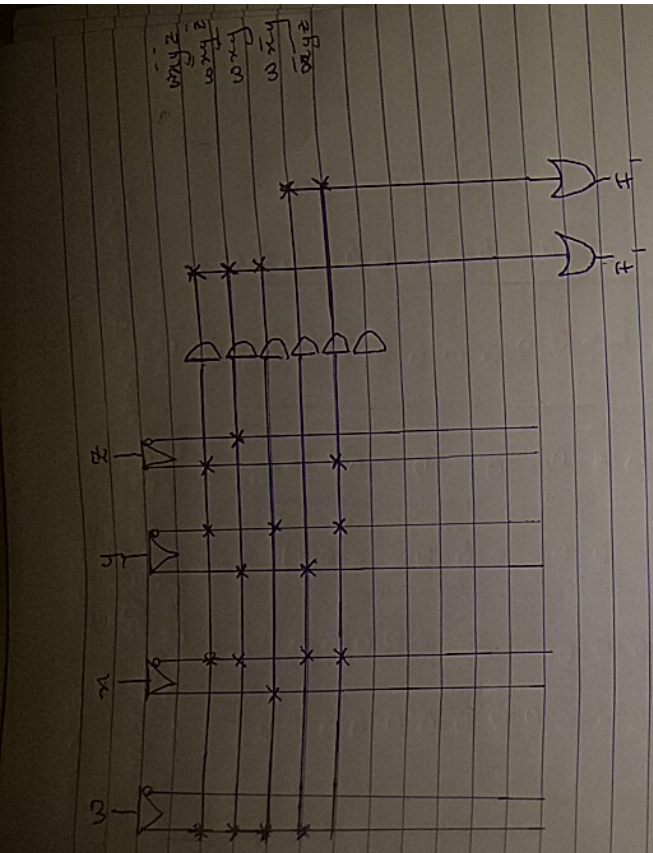
$F_1(w, x, y, z) = wx'y + wx'yz' + wxy'$

$F_2(w, x, y, z) = wx'y + x'y'z$

w	x	y	z	F_1	F_2
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	0	1	1	1
1	0	1	0	1	0
1	0	1	1	0	0
1	1	0	0	1	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0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