**HASHIM ABDULHADI**

**16/ENG02/062**

**COE 506**

**DIGITAL SYSTEM DESIGN USING VHDL**

**ASSIGNMENT SOLUTION**

**QUESTION 1**

1. ASIC -**Application Specific Integrated Circuits**
2. PAL- **Programmable Array Logic**
3. PLA-**Programmable Logic Array**
4. PLD- **Programmable Logic Device**
5. CPLD- **Complex Programmable Logic Device**
6. FPGA- **Field-Programmable Gate Array**

**QUESTION 2**

Higher granularity level directly decreases time delay between the input and the output. It decreases the delay in critical path. However, the average fan out increases and the number of switches also increases as each block has more pins. Wire length also increases as the size of blocks increase.

**QUESTION 3**

PLC are preferable to hard wiring because they offer:

1. Accuracy
2. Simplicity
3. Cost efficient

**QUESTION 4**

The stored program will be nonvolatile, and it would also be read-only. For this reason, fuse-programmed devices are also called OTP ( one time programmable) which means that it’s a type of of non-volatile memory (NVM) which permits data to be written to memory once. It retains its value upon loss of power once it has been written. It is used in applications where reliability and multiple data read is needed.

