**SUMMARY OF THE NOTES**

An analog multiplier in electronics is a system that takes two analog signals, and generates an output that is their product.

In analog multiplier, nonlinear operations on continuous signals are required. The operations include rectification, modulation, demodulation, frequency translation, multiplication and division.



Where V is thermal voltage, and where the base currents are ignored. Combining above, the gap between the two outputs as



The relationship is plotted and reveals that a coupled pair of emitters can be used as a primitive multiplier by itself.



The assumption that Vid is small and that Vi2 is greater than VBE(on), we created a circuit that acts as a multiplier. This multiplier also functions in only two quadrants of Vid-Vi2 plane, that’s why it is termed a two-quadrant multiplier.

A method called Gilbert multiplier cell is also an emitter-coupled cell modification but allows the multiplication of four quadrants. Consequently, it forms the basis for most integrated circuit balanced multipliers. The structure of the Gilbert multiplier cell is formed by two cross-coupled emitter coupled pairs in series connection with an emitter coupled pair.



 The equations are:

The collector current of Q3 and Q4 are given by



Similarly, the Q5 and Q6 collector current is given by the



The current collector IC1 and IC2 of the Q1 and Q2 transistors can be expressed as



We get the above equation substituted in IC3 and IC4



In the same way, we substitute Ic2= in Ic5 and IC6,



The differential output current I is given by

∆I =IL1 - IL2

= (IC3 +IC5) - ( IC4+IC6)

=IC3 - IC6)-(IC4 - IC5)

∆I=IEE tanh( V1/2VT) tanh(V2/2VT)

Gilbert cell can also be used as a Balanced Modulator; a need also occurs for a constantly changing signal to be multiplied by a square wave. It is conveniently achieved by adding a sufficiently large signal directly to the cross-coupled pair with the circuit multiplier. The spectrum of the modulation has a component located at frequencies ωm above or below the harmonics of ωc which has no component at the carrier frequency, there is also lack of an output component at the carrier frequency which is very useful for balanced modulators.

Gilbert cell can also be used as a phase detector, the circuit serves as the phase detector and results in a dc component which is proportional to the phase difference between the two incoming signals, if unmodulated signals of the same frequency correspond to the two inputs.

 **phase lock loop (PLL)**

The phase lock loop (PLL) is a control system that generates an output signal, the phase of which relates to the input signal phase. The phase lock loop is also a control system that allows an oscillator to track another oscillator. A phase difference between input and output is possible, but when looked, frequencies will be tracked.

Phase-locked loop mechanisms may be implemented as either analog or digital circuits. Both implementations use the same basic structure. Analog PLL circuits include four basic elements:

* Phase detector,
* Low-pass filter,
* Voltage controlled oscillator, and
* feedback path (which may include a frequency divider).

Some applications of the phase locked loop are:

* frequency synthesizer
* clock recovery in serial data link
* clock generation
* Demodulation of frequency modulation (FM)
* Demodulation of frequency-shift keying (FSK)
* DC motor drive

 **BLOCK DIAGRAM OF THE PROCESSES IN PHASE LOCKED LOOP**

Phase

detector

Loop

filter

VCO

φ

in

(

t

)

ω

in

(

t

)

φ

out

)

(

t

ω

out

(

t

)

v

e

(

t

)

V

cont

**A phase detector** is a frequency, analog or logical circuit that provides a tension signal, representing the difference between phase inputs of two signal points.

KD is the gain of the phase detector (V/rad).

 ve(t) = KD[φout(t) − φin(t)]

**A voltage-controlled oscillator (VCO)** is an electronic oscillator whose oscillation frequency is controlled by a voltage input. The applied input voltage defines the instantaneous oscillation frequency. As a result, a VCO is usable with the use of a modulating signal for frequency modulation (FM) or phase modulation (PM). A VCO is also a part of a locked-phase loop.

t φout = KO ∫Vcont dt' −∞

A finite VCont is required in order to achieve an arbitrary output frequency (naturally within the VCO tuning range). Let's say φout – φin = φο.



The two inputs to the detector are shown as square waves in the figure above. If there is a phase misalignment, the XOR function produces an output pulse. Suppose a frequency of output < 1 is necessary. From the figure above right we see that this output frequency needs a control voltage V1. Only by holding a phase offset −0 input can the Phase Detector generate this V1. The PLL loop gain, KD KO, should be maximized to minimize the necessary phase offset or error.

**LOCK RANGE:** it is the reference range of signal frequencies that the loop is locked after the input signal has been captured. The phase detector or the VCO frequency range can restrict this.

π/2

π

φ

K

D

π/2

-

K

D

π/2

V

e

From the diagram the active range where lock can be maintained is 0 < φ < π. In the opposite direction, the frequency will change to that needed to sustain the locked state.

Ve-max = ± KD π/2

## When the output voltage of the phase detector is applied by the VCO loop filter,

## ∆ωout – max = ± KV π/2 = ωL (lock range)

Where kv=KoKD, which is the product of the phase detector and the vco gain.

It is the spectrum of frequencies around the loop's free running frequency.

Does not depend on the loop filter depends on the gain of the DC loop.

**Capture range:** it is the range of input frequencies around the VCO core frequency that the loop locks to when the condition begins. Initial locking can be aided by connecting a frequency detector to the phase sensor.

**Bandwidth.** For noise purposes the 3 dB bandwidth loop is significant. The bandwidth is calculated by both −n and −n, so the bandwidth needs to be measured in accordance with the overhead and time settings. Also, in the case of a forward path zero, we find that the formula varies from feedback zero.

ω*h* =ω3*dB* =ω*n* [1+ 2ζ2 + (2ζ2 +1)2 +1]

ω3db = 2 ωn for ζ = 0.707

ω3db = 2.5 ωn for ζ = 1

As the loop reaches peak and exceeds zero, as this shows, we also expect bandwidth to be higher. We see that the response to frequencies is small. The phase noise of the reference source is then transferred through the PLL and filtered, as in the figure shown. 2 or 3. We have no input noise attenuation under the 3 dB range. Above, 40 dB / decade eliminates the noise. Note also that gain peak for < 2 is open. The advantage of Type II CP PLL or PLL opamp filter is also that the zero frequency in the highly damp case is always lower than the pole frequency.

**Third-order CP PLL**: One outstanding question is still ignored. This phase detector produces pulses of variable width to either load or unload the CP condenser. Furthermore, once we have the resistor attached, the control voltage from the charging pump bounces up or down before achieving its constant status. The truth remains that the voltage cannot be modified instantaneously through the condenser, which makes the initial voltage fall from RP and exponentially charges CP. This jumpy frequency modulates the VCO and induces reference spurs at the reference frequency.

The bandwidth also plays a role in the PLL noise behavior which have 2 main sources

1. Reference noise:

|  |  |
| --- | --- |
| φ*out* φ*ref* |  *Forward Path K*= = *V F*(*s*)/*s*   1+*T*(*s*) 1+ *KV F*(*s*)/ *Ns* |

= *Ns*2*N*/*K*(1*V*++*ss*/ω/ω2)2 +1

1. VCO noise: φ*out* = *Forward Path* = 1

 φ*vco* 1+*T*(*s*) 1+ *KV F*(*s*)/ *Ns*

 = 2 /*NsKV*2+/*Ks V*/ω2 +1

## Ns