Analog multipliers

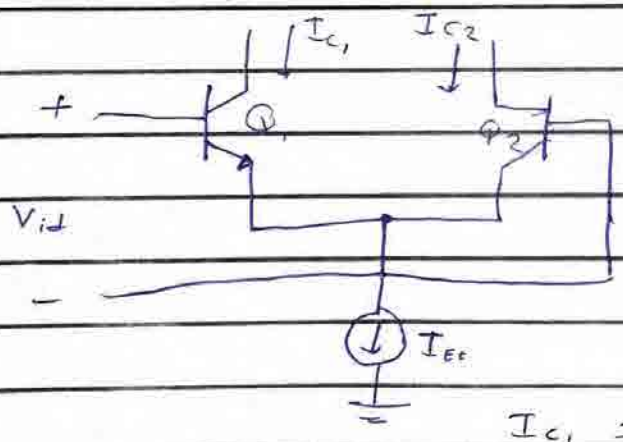
Non-linear operations include

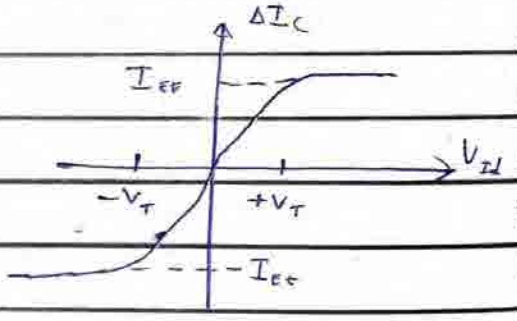
- rectification
- modulation
- demodulation
- frequency translation
- multiplication and
- division

These operations on continuous-valued analog signals are required in instrumentation, communication and control system design.

Analog multiplier: Circuit taking two analog inputs and producing an output proportional to their product.

Emitter-coupled pair as a simple multiplier





$$I_{C1} = \frac{I_{EE}}{1 + \exp(-V_{id}/V_T)}$$

$$I_{C2} = \frac{I_{EE}}{1 + \exp(V_{id}/V_T)}$$

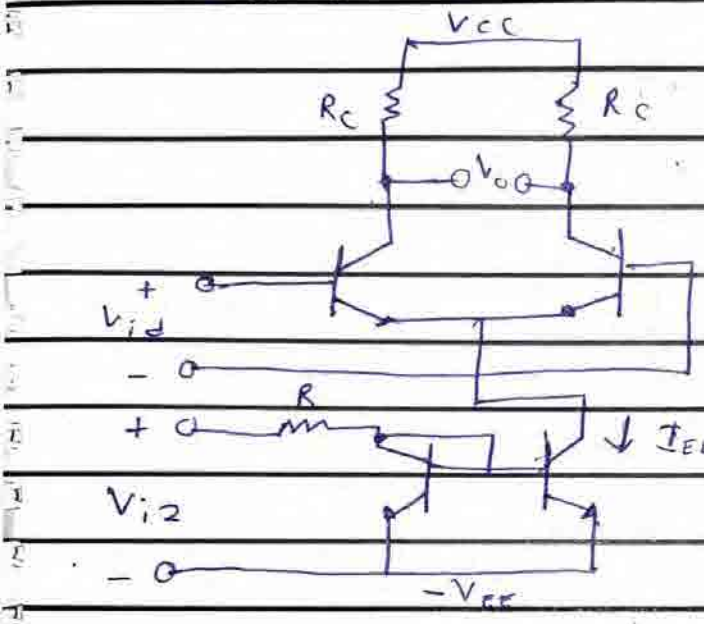
$$\Delta I_C = I_{C1} - I_{C2} = I_{EE} \tanh(V_{id}/2V_T)$$

This configuration (emitter coupled pair) can be used as a primitive multiplier

If $\frac{V_{id}}{2V_T} \ll 1 \Rightarrow \Delta I_c = I_{EE}\left(\frac{V_{id}}{2V_T}\right)$

I_{EE} - bias current for the emitter-coupled pair

Adding an additional circuit



$I_{EE} \cong k_0(v_{i2} - V_{BE(on)})$

$\downarrow I_{EE}$ $\Delta I_c \cong \frac{k_0 V_{id}(v_{i2} - V_{BE(on)})}{2V_T}$

Two quadrant restriction

The above function as a multiplier under the assumption that V_{id} is small and $V_{i2} > V_{BE(on)}$

↓

multiplier function is only to a (two-quadrant multiplier)

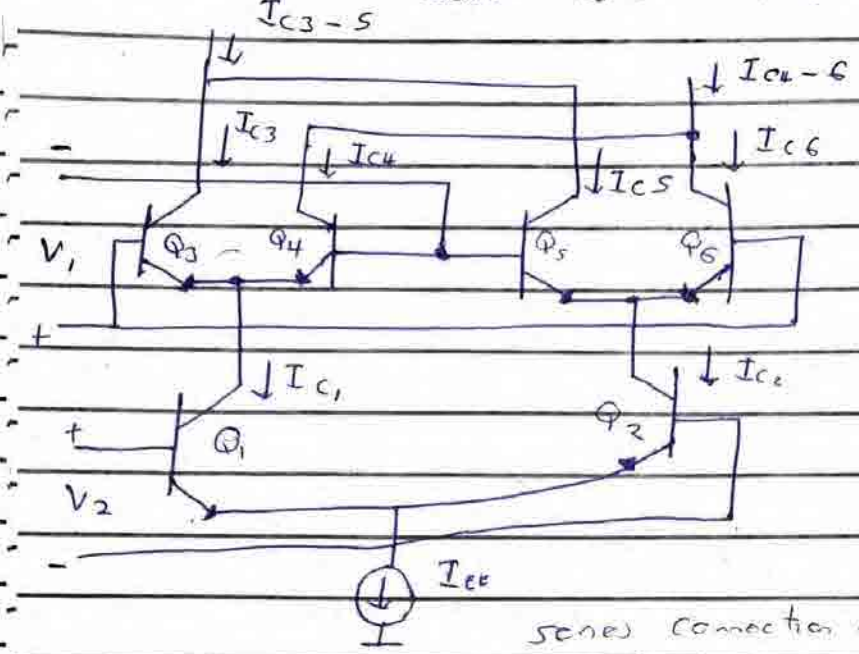
quadrants of the $V_{id} - V_{i2}$ plane

most practical multipliers allow four-quadrant operation

Gilbert multiplier cell

It is a modification of the emitter-coupled cell, allowing four-quadrant multiplication. It is the basis for most integrated circuit balanced multiplier systems

$I_{out} = I_{C3-5} - I_{C4-6}$



series connection of an emitter-coupled pair with two cross-coupled, emitter-coupled pairs

$$I_{C3} = \frac{I_{C1}}{1+\exp(-V_1/V_T)} \qquad I_{C4} = \frac{I_{C1}}{1+\exp(V_1/V_T)}$$

$$I_{C5} = \frac{I_{C2}}{1+\exp(V_1/V_T)} \qquad I_{C6} = \frac{I_{C2}}{1+\exp(-V_1/V_T)}$$

$$I_{C1} = \frac{I_{EE}}{1+\exp(-V_2/V_T)} \qquad I_{C2} = \frac{I_{EE}}{1+\exp(V_2/V_T)}$$

I_{C3}, I_{C4}, I_{C5}, and I_{C6} can be related to V_2 by substituting either I_{C1} or I_{C2} as the case may be

The differential output current is given by

$$\Delta I = I_{C3-5} - I_{C4-6} = I_{C3} + I_{C5} - (I_{C4} + I_{C6})$$
$$= (I_{C3} - I_{C6}) - (I_{C4} - I_{C5})$$
$$= I_{EE} \tanh(V_1/2V_T) \tanh(V_2/2V_T)$$

Applications of Gilbert Cell

1) If $V_1 < V_T$ and $V_2 < V_T \Rightarrow \tanh(V_{1,2}/2V_T) \simeq V_{1,2}/2V_T$

it works as a MULTIPLIER

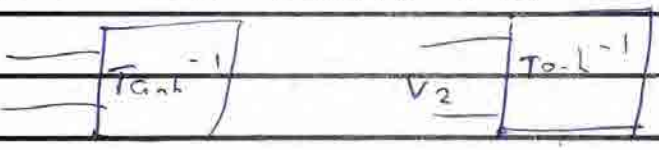
2 If one of the inputs is large compared to V_T, the applied signal is multiplied by a ~~small~~ square wave. Acts as a MODULATOR

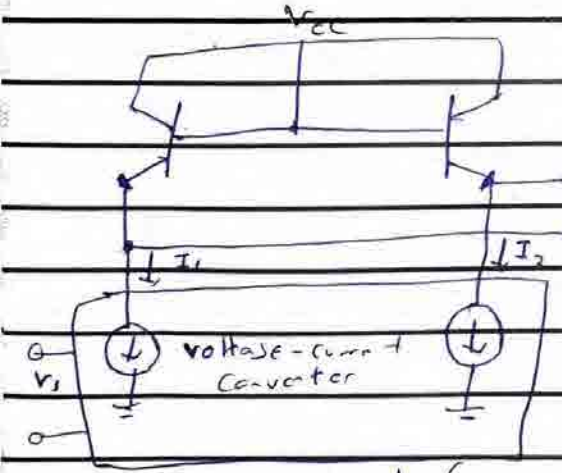
3 If both inputs are large compared to V_T, transistors behaving as nonsaturating switches. It is useful for phase difference detection required in phase-locked loops (Phase-detector mode

Gilbert cell as a multiplier

$V_1 < V_T$, $V_2 < V_T$ $\Rightarrow \tanh(x) = x + x^3/3 + \cdots \approx x$

An inverse hyperbolic tangent nonlinearity is used to predistort the input signals to compensate for the hyperbolic tangent transfer characteristics





$I_1 = I_{01} + k_1 V_1$, $I_2 = I_{01} - k_1 V_1$

I_{01} is the dc current that flow in each output leal if V_1 is equal to zero. and k_1 is the transconductance of the voltage-to-current Converter

$$\Delta V = V_T \ln\left(\frac{I_{01} + k_1 V_1}{I_S}\right) - V_T \ln\left(\frac{I_{01} - k_1 V_1}{I_S}\right)$$

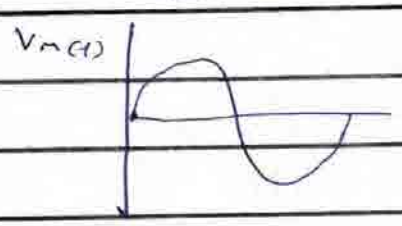
$$= V_T \ln\left(\frac{I_{01} + k_1 V_1}{I_{01} - k_1 V_1}\right)$$

Using $\tanh^{-1} x = \ln\left((1+x)(1-x)\right)/2$

$$\Delta V = 2 V_T \tan^{-1}\left(\frac{k_1 V_1}{I_{O1}}\right) \qquad \Delta I = I_{EE}\left(\frac{k_1 V_1}{I_{O1}}\right)\left(\frac{k_2 V_2}{I_{O2}}\right)$$

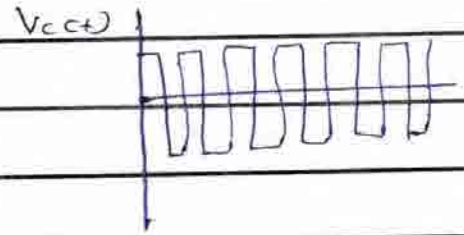
$$V_{out} = I_{EE} k_3 \frac{k_1}{I_{C1}} \frac{k_2}{I_{O2}} V_1 V_2 = 0.1 V_1 V_2$$

Gilbert cell as a balanced modulator



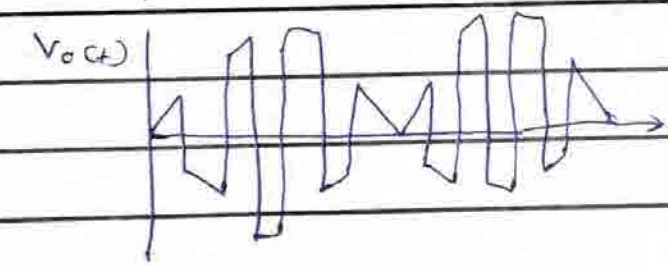
$$V_m(t) = V_m \cos \omega_m t$$

$$V_c(t) = \sum_{n=1}^{\infty} A_n \cos n\omega_c t \qquad A_n = \frac{\sin\left(\frac{n\pi}{2}\right)}{\frac{n\pi}{4}}$$



$$V_o(t) = k\left(V_c(t) V_m(t)\right)$$

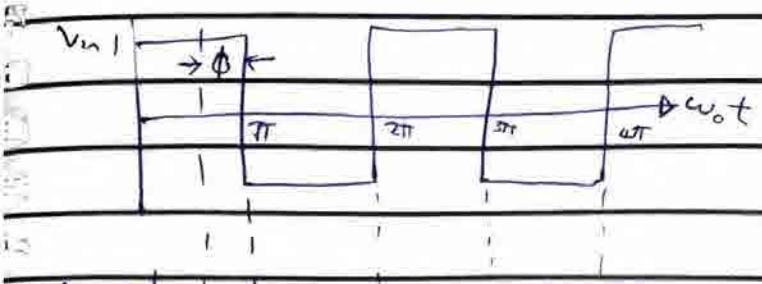
$$= k \sum_{n=1}^{\infty} A_n V_m \cos \omega_m t \cos n\omega_c t$$

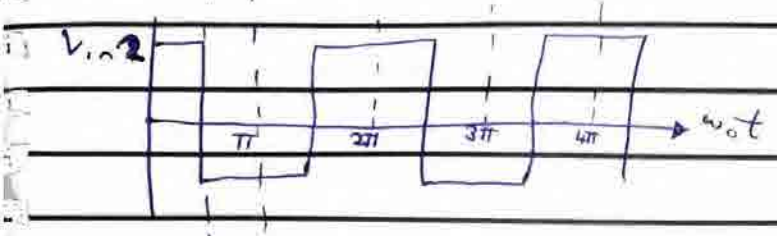


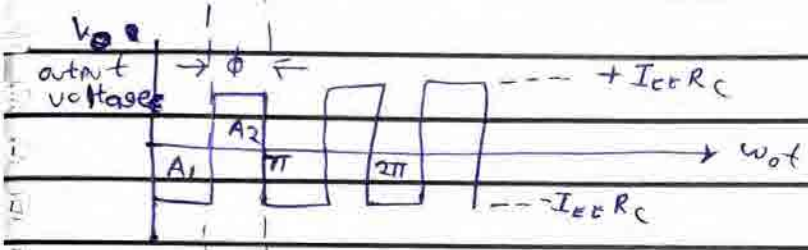
$$= k \sum_{n=1}^{\infty} \frac{A_n V_m}{2} \cos\left(n\omega_c t - \omega_m t\right) \cos\left(n\omega_c t + \omega_m t\right)$$

Gilbert cell as a phase detector

If unmodulated signals of identical frequency are applied to the two inputs, the circuit behaves as a phase detector producing an output whose dc component is proportional to the phase difference between the two inputs







The DC component is given by

$$V_{average} = \frac{1}{2\pi}\int_0^{2\pi} V_0(t)\, d(\omega_0 t)$$

$$= \frac{-1}{\pi}\left[A_1 - A_2\right]$$

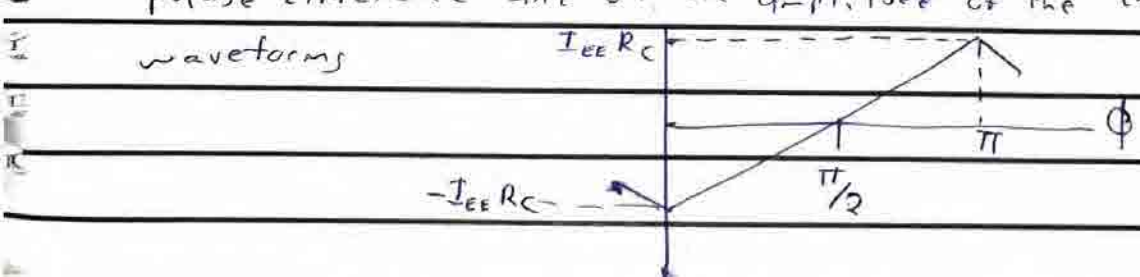
A_1 and A_2 are surface areas

$$V_{average} = -\left[\frac{I_{EE}R_C\,\pi - \varphi}{\pi} - \frac{I_{EE}R_C\,\varphi}{\pi}\right]$$

$$= I_{EE}R_C\left(\frac{2\varphi}{\pi} - 1\right)$$

The circuit still acts as a phase detector if the inputs are comparable to or smaller than V_T

The output voltage then depends both on the phase difference and on the amplitude of the two input waveforms

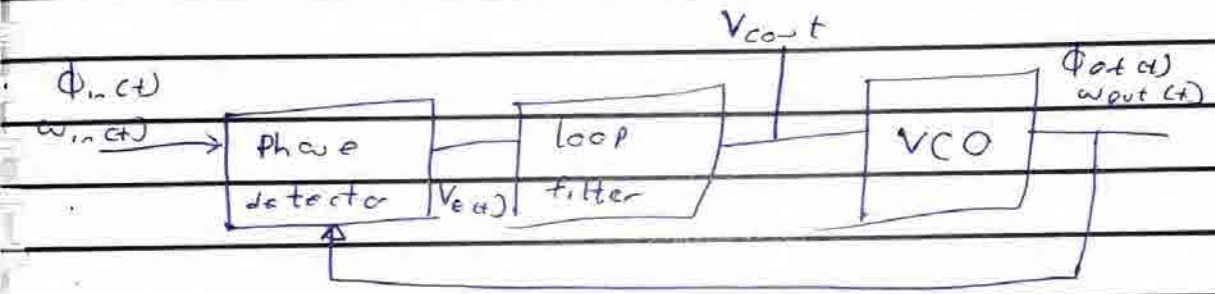


PLL

1) Definition: A PLL is a feedback system that includes a VCO, phase detector and low pass filter within its loop. It forces the vco to replicate and track the frequency and phase at the input when in lock. Phase offset may exist between input and output but frequencies must track when locked

$$\Phi_{out}(t) = \Phi_{in}(t) + const$$

$$\omega_{out}(t) = \omega_{in}(t)$$



The PLL output can be taken from either V_{cont} (filtered VCO control voltage or from the VCO's output. The former provides a baseband output that tracks the phase variation at the input while the vco output is used as a local oscillator or to generate a clock signal for a digital system

$$\omega(t) = \frac{d\phi}{dt} \Rightarrow \phi(t) = \phi(0) + \int_0^t \omega(t')\,dt$$

Application

- clock generation
- frequency synthesis
- Clock recovery in a serial data link

phase detector : Generates an error signal $V_e(t)$ proportional to the phase difference between the two inputs. It has a gain k_D (V/rad)

$$V_e(t) = k_D [\phi_{out}(t) - \phi_{in}(t)]$$

3 VCO : In PLL applications, the VCO is treated as a linear, time-invariant system. Excess phase of the VCO is the system output

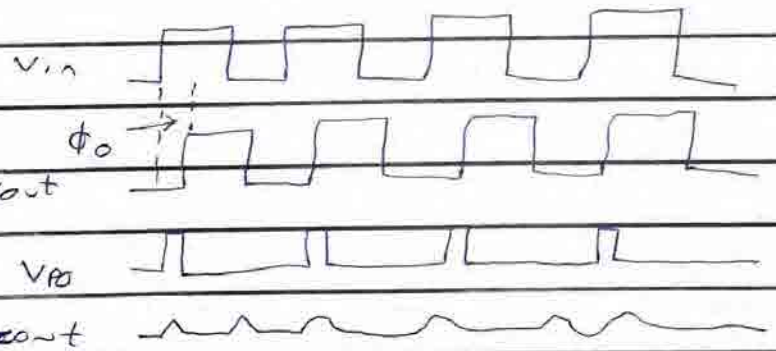
$$\phi_{out} = k_o \int_{-\infty}^{t} V_{cont}\, dt'$$

The VCO oscillates at an angular frequency, ω_{out} when control voltage is zero, frequency is nominal ω_o

$$\omega_{out} = \omega_o + k_o V_{cont}$$

k_O - gain coefficient

$\phi_{out} - \phi_{in} = \phi_o$



4 PLL dynamic response

A temporary change in frequency is necessary to shift the phase by ϕ_1, The area under ω_{out} gives the additional phase because $V_{cont} \propto$ frequency

$$\phi_1 = \int_{t_1}^{\infty} \omega_{out}\, dt = \int_{t_1}^{\infty} k_o V_{cont}(t)\, dt$$

The initial and final frequencies are the same, so $V_{cont}(t)$ can be used to monitor the dynamic phase

response of the PLL

$$\omega_2 = \omega_1 + \Delta\omega$$

5 Lock range: This is the range of input signal frequencies over which the loop remains locked once it has captured the input signal. It can be limited by the phase detector or the VCO frequency range

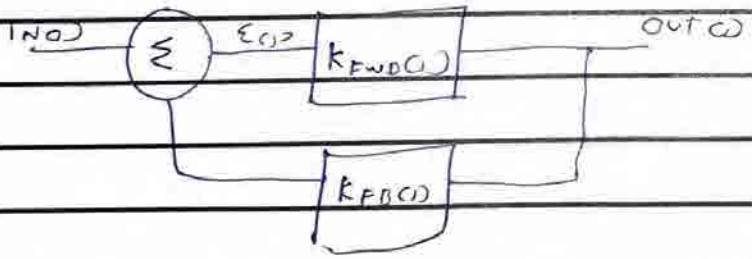
6 Capture range: range of input frequencies around the VCO center frequency at which the loop will lock when starting from an unlocked condition

7 Approach: Assuming the PLL is a linear feedback system and using a frequency domain approach

$$\frac{V_E(s)}{\Delta\phi} = k_D$$

$$\frac{\phi_{out}(s)}{V_{cont}(s)} = \frac{k_0}{s}$$

PLL is a feedback system



Loop gain $T(s) = k_{FWD}(s)\, k_{FB}(s)$

Transfer function: $\frac{OUT(s)}{IN(s)} = H(s) = \frac{k_{FWD}(s)}{1 + T(s)}$

Loop gain is a polynomial

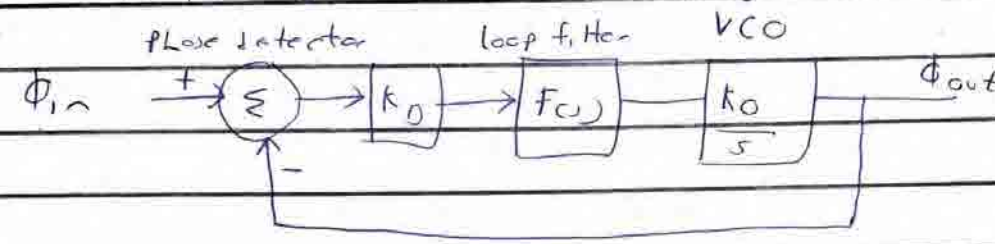
$$T(s) = \frac{k'(s+a)(s+b)\cdots}{s^n (s+\alpha)(s+\beta)}$$

phase error $= \varepsilon(s) = \dfrac{N(s)}{1 + T(s)}$

steady state error $= \varepsilon_{ss} = \lim_{s \to 0} [s\varepsilon(s)] = \lim_{t \to \infty} \varepsilon(t)$

A large loop gain leads to a small phase error

frequency and phase tracking loop



$H(s) = \dfrac{\text{forward path gain}}{1 + T(s)}$

feedback $= 1$

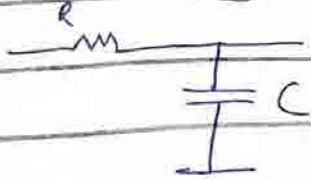
$H(s) = \dfrac{T(s)}{1 + T(s)} \Rightarrow H(s) = \dfrac{\phi_{out}}{\phi_{in}} = \dfrac{K_0 K_0 F(s)/s}{1 + K_0 K_0 F(s)/s}$

Phase error function $\varepsilon_s = \phi_{in} - \phi_{out} = \dfrac{s\phi_{in}}{s + K_0 K_0 F(s)}$

Open loop gain $T(s)$

$T(s) = K_0 F(s) \dfrac{K_0}{s}$

Since the phase detector produces an output equal to or at twice the carrier frequency, low pass filtering will be needed. Using an RC lowpass network



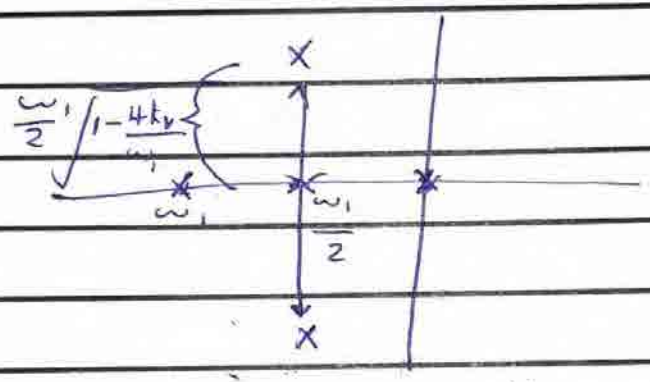
The network has a cutoff (3 dB) frequency $\omega_1 = \dfrac{1}{RC}$

Root locus

$$1 + T(s) = 0$$

$$s = -\frac{\omega_1}{2}\left(1 \pm \sqrt{1 - \frac{4k_v}{\omega_1}}\right)$$

as k_v increases, the roots approach one another then became complex conjugate.

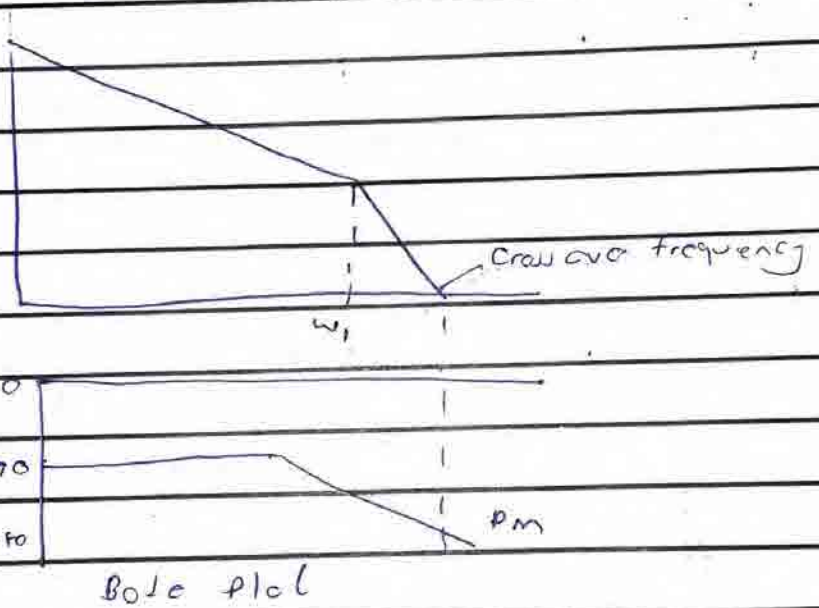


The filter transfer function is a simple low pass

$$F(s) = \frac{1}{1 + \frac{s}{\omega_1}}$$

$$\Rightarrow T(s) = \frac{k_0}{s} \frac{k_D}{1 + \frac{s}{\omega_1}} = \frac{k_V}{s(1 + s/\omega_1)}$$

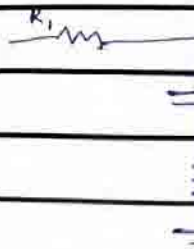
$k_V = k_0 k_D$



Bode plot

If the loop filter frequency is lower than the crossover frequency (to attenuate the High Frequency ripple from the phase detector) the phase margin can become unacceptably small. If we increase the loop gain k_V, $k_0 k_D$ to reduce the residual phase error, we get even smaller phase margin.

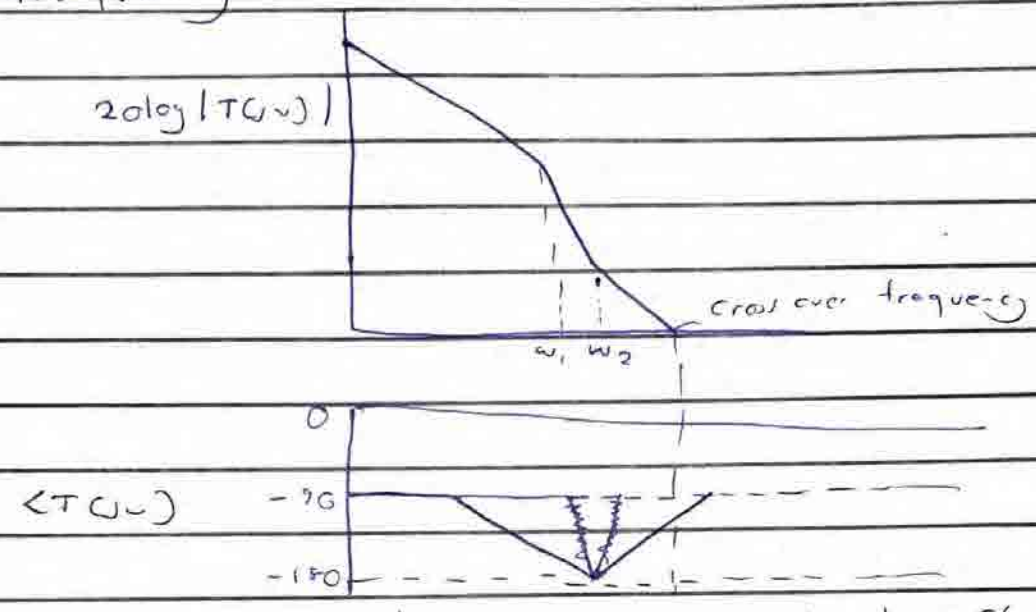
Adding a resistor to the low pass loop filter contributes a zero to its transfer function



$$F(s) = \frac{1 + \frac{s}{\omega_2}}{1 + \frac{s}{\omega_1}}$$

$\omega_1 = \frac{1}{(R_1 + R_2)C}$ $\omega_2 = \frac{1}{R_2 C}$

Zero frequency is always higher than the pole frequency



The phase margin be increased, small values of ω_1 can be used for narrower filter bandwidth or higher k_v value can be used for lower phase error without sacrificing phase margin

phase error

no frequency error when the loop is locked

Input frequency = output frequency

but phase error may exist; the phase error must remain bounded in order to keep the loop locked

Phase error $= \varepsilon(s) = \frac{N(s)}{1 + T(s)}$

steady state error $\varepsilon_{ss} = \lim_{s \to 0} [s\varepsilon(s)] = \lim_{t \to \infty} \varepsilon(t)$

$\varepsilon(s) = 20\log\left(\frac{\phi_{out}}{\phi_{in}}\right)$ dB

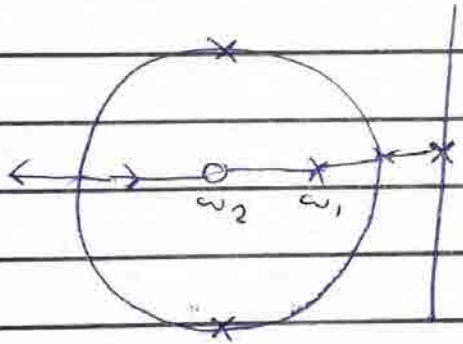
Root locus

$$\frac{\Phi_o}{\Phi_{in}} = \frac{1 + s/\omega_2}{\frac{s^2}{k_v \omega_1} + s\left(\frac{1}{k_v} + \frac{1}{\omega_2}\right) + 1}$$

$$\omega_n = \sqrt{k_v \omega_1}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{k_v}} + \frac{1}{2}\frac{\omega_n}{\omega_2}$$

$$s = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$$



The phase error increases as the input frequency approaches the natural loop frequency for the case with $\zeta = 0.707$ (damping coefficient)

Transient phase error

- Inverse laplace transform of $\varepsilon(s)$

The phase error is affected by the type of transient phase signal at the input

1) phase step

$$\phi_{in}(t) = \Delta\theta\, u(t)$$

$$\phi_{in}(s) = \frac{\Delta\theta}{s}$$

steady-state phase error can be calculated from $\varepsilon(s)$ and ε_{ss} above

$$\varepsilon_{ss} = \lim_{s\to 0} \frac{s\frac{\Delta\theta}{s}}{1 + \frac{k_v}{s}\left(\frac{1+\frac{s}{\omega_2}}{1+\frac{s}{\omega_1}}\right)} = 0$$

There is only a transient phase error for a phase step

2 frequency step

$$\varepsilon_{ss} = \lim_{s\to 0} \frac{s\frac{\Delta\omega}{s^2}}{1 + \frac{k_v}{s}\left(\frac{1+s/\omega_2}{1+s/\omega_1}\right)}$$

$$= \lim_{s\to 0} \frac{\Delta\omega}{s + k_v\left(\frac{1+\frac{s}{\omega_2}}{1+\frac{s}{\omega_1}}\right)} = \frac{\Delta\omega}{k_v}$$

The static error can be made small by increasing k_v

3 frequency ramp (Doppler shift) : An unlimited steady state error is obtained. Type 1 system is not suitable for a fast moving object

Summarising for a Type 1; second order system

$$F(s) = \frac{1 + \frac{s}{\omega_2}}{1 + \frac{s}{\omega_1}}$$

Input	$\phi_{in}(s)$	ε_{ss}
phase step	$\Delta\phi / s$	0
Freq. step	$\Delta\omega / s^2$	$\Delta\omega / K_v$
Freq ramp	A / s^2	Infinite

Type 2; second order $F(s) = \frac{1 + \frac{s}{\omega_2}}{s/\omega_1}$

Input	$\phi_{ref}(s)$	ε_{ss}
phase step	$\Delta\theta / s$	0
Freq. step	$\Delta\omega / s^2$	0
Freq. ramp	A / s^2	kA

placing an opamp RC integrator or charge pump in the loop

$$F(s) = \frac{1 + s/\omega_2}{s/\omega_1}$$

providing a pole at $s = 0$ and a zero at ω_2.

Then the loop gain $T(s)$ will be that of a type 1 Control system

$$T(s) = \frac{k_0 k_o \left(1 + \frac{s}{\omega_2}\right)}{s^2/\omega_1}$$

Closed loop transfer function

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{k_0 k_o F(s)/s}{1 + k_0 k_o F(s)/s}$$

$$H(s) = \frac{\left(1 + s/\omega_2\right)}{\frac{s^2}{k_0 k_o \omega_1} + \frac{s}{\omega_2} + 1}$$

$$\Rightarrow \omega_n = \sqrt{k_0 k_\Delta \omega_1}$$

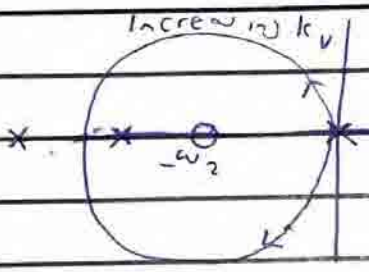
$$\zeta = \frac{\omega_n}{2\omega_2}$$

Root locus

finding poles of $1 + T(s) = 0$ let $k_v = k_0 k_\Delta$

$$\frac{s^2}{k_v \omega_1} + \frac{s}{\omega_2} + 1 = 0$$

$$s = \zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$$



As the loop gain k_v increase both real and imaginary parts grow. locus follows a circle Centered around the zero. The poles become real again at $\zeta = 1$ it happens when

$$k_v = \frac{4\omega_2^2}{\omega_1}$$

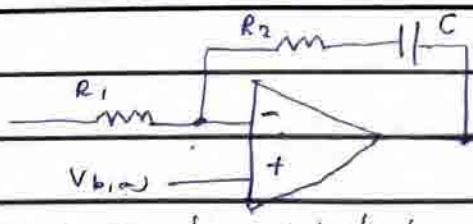
Bandwidth

$$\omega_b = \omega_{3dB} = \omega_n\left[1 + 2\zeta^2 + \sqrt{(2\zeta^2+1)^2 + 1}\right]^{1/2}$$

$\omega_{3dB} = 2\omega_n$ for $\zeta = 0.707$

$\omega_{3dB} = 2.5\omega_n$ for $\zeta = 1$

Loop filter - OP Amp



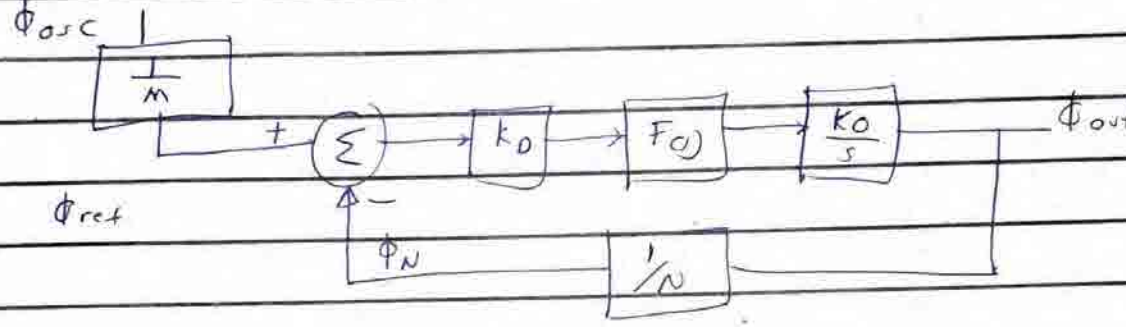
The op-a-p Can be used to form a filter that includes a pole at $s = 0$ and a finite zero

$$F(s) = \frac{V_{out}}{V_{in}} = \frac{1 + sR_2C}{sR_1C}$$

V_{bias} can be used to level shift between the phase detector and the VCO

Synthesizer PLL

Adding the divider $\frac{1}{N}$ to the feedback path



$$\frac{\phi_N}{\phi_{out}} = \frac{1}{N} \qquad N = \frac{\omega_{out}}{\omega_{ref}}$$

$$T(s) = \frac{K_D K_O F(s)}{N_s}$$ loop gain is reduced by a factor N

N is not a constant in most applications

$K_V = K_D K_O$ is not a constant - varies with frequency according to N

$$F(s) = \frac{1 + s/\omega_2}{s/\omega_1} \qquad \omega_1 = \frac{1}{R_1 C}$$

$$\omega_2 = \frac{1}{R_2 C}$$

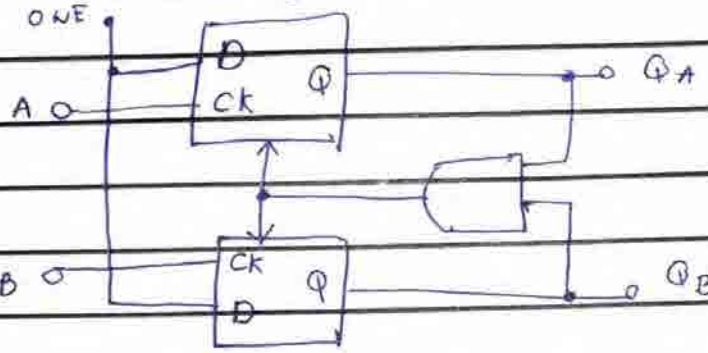
$$1 + T(s) = 1 + \frac{K_V}{N_s}\left(\frac{1 + s/\omega_2}{s/\omega_1}\right) = 0$$

$$1 + T(s) = \frac{N s^2}{K_V \omega_1} + \frac{s}{\omega_2} + 1 = 0$$

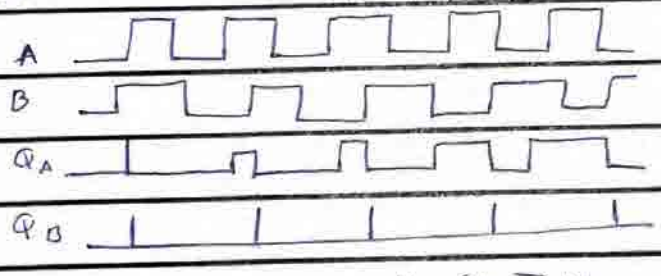
$$\omega_n = \sqrt{\frac{K_V \omega_1}{N}} = \sqrt{\frac{K_V}{R_1 C N}}$$

$$\zeta = \frac{\omega_n}{2\omega_z} = \frac{R}{2}\sqrt{\frac{k_v C}{R_1 N}}$$

Phase frequency Detector

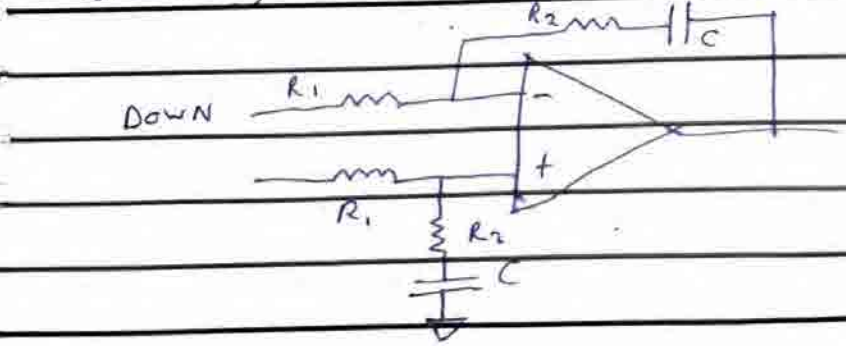


The phase-frequency detector above is a widely used architecture in frequency synthesizers



Circuit response with $\omega_A \geq \omega_B$

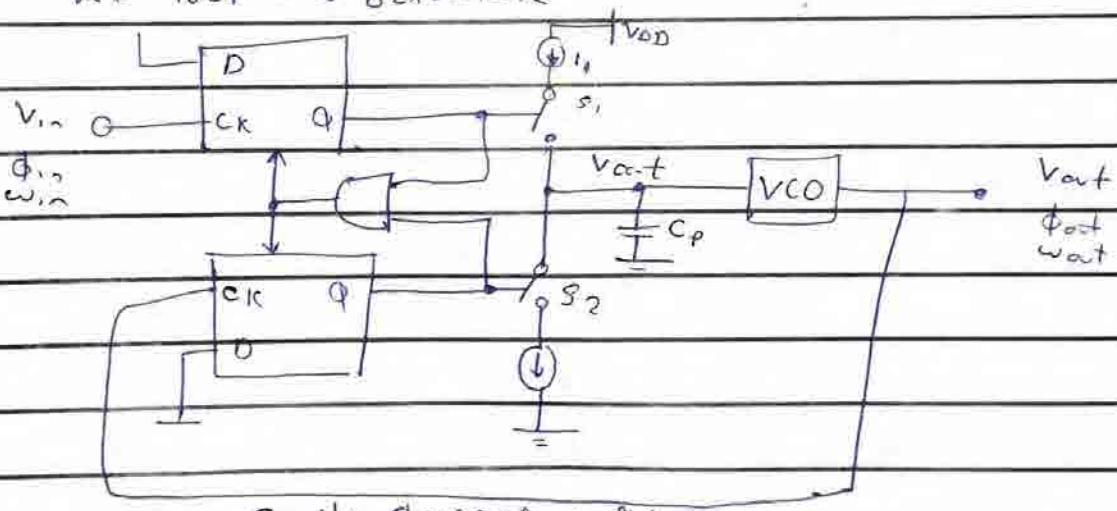
The phase detector has a much larger phase range (4π) of operation and it will produce an output that drives the frequency in the right direction when it is out of lock



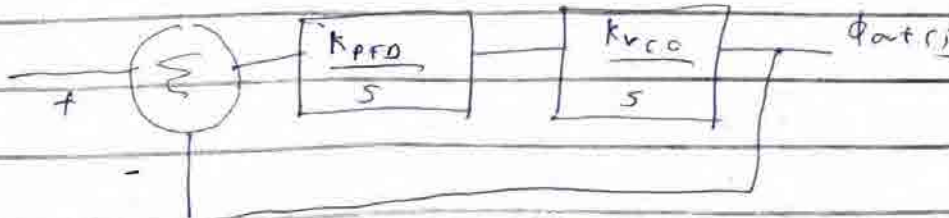
Charge Pump loop filter

Very convenient to implement in CMOS

- The PFD output produces Up (Q_A) and Down (Q_B) pulses whose width is proportional to the phase error
- Charge Pump current sources I_1 must be equal to I_2 charging and discharging the capacitor C_p in discrete steps
- If there is a static phase error $\Delta\phi$ at the PFD input the capacitor C will be charged indefinitely — DC gain is infinite: Ideal integrator with zero static phase error
- The CP PLL will detect small phase errors and correct them as long as the frequency of the phase error is within the loop 3dB bandwidth



Simple charge-pump PLL



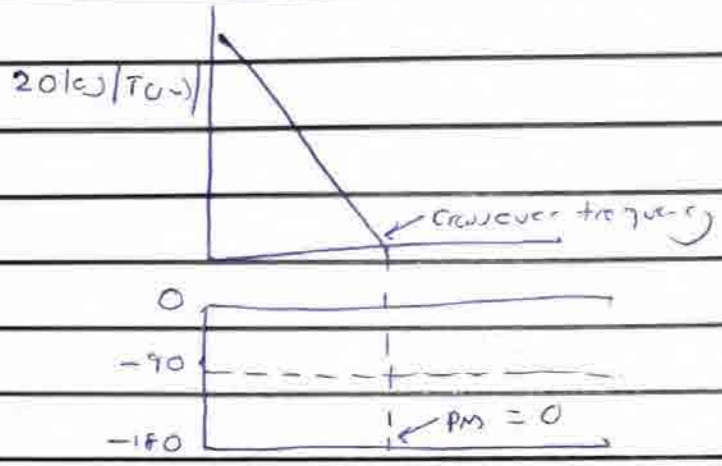
← PFD/CP/LPF → ← VCO →

$$T(s) = \frac{K_{PFD}}{5} \frac{K_{VCO}}{5}$$

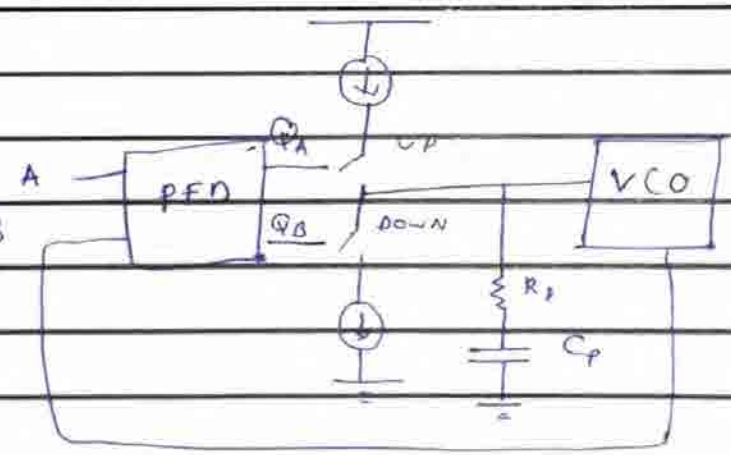
T(s) has a factor of s^2 in the denominator

(Type II loop)

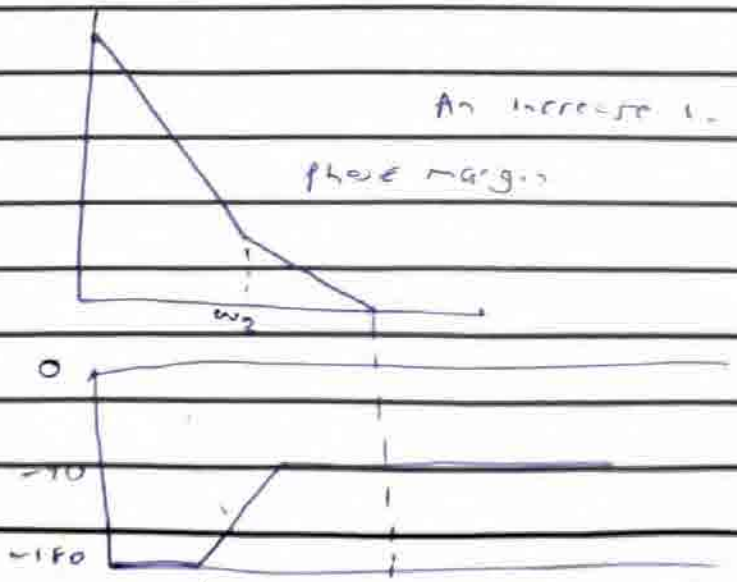
Phase margin is always zero

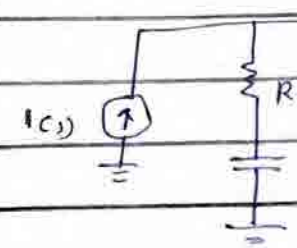


To provide some phase lead to stabilise the PLL, a zero must be added to the loop filter T.F



An increase in loop gain improves phase margin





$$H(s) = \frac{V_{out}(s)}{\Delta\phi} = \frac{I_p}{2\pi} \frac{1}{C_p s} = \frac{k_{PFD}}{s}$$

$$I(s) = \frac{V_{out}(s)}{Z(s)} = \frac{V_{out}(s)}{\frac{1}{sC_p}}$$

$Z(s)$ is the complex impedance

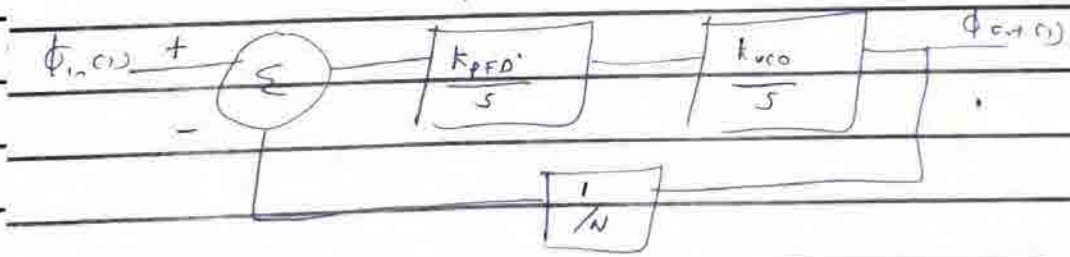
$$\frac{I(s)}{\Delta\phi} = \frac{I_p}{2\pi}$$

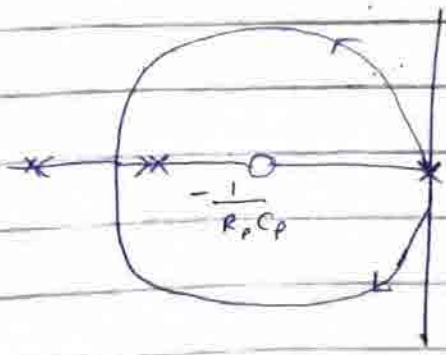
replace $\frac{1}{sC_p}$ with $Z(s) = R_p + \frac{1}{sC_p}$

$$\frac{V_{out}}{\Delta\phi} = \frac{I_p}{2\pi}\left(R_p + \frac{1}{sC_p}\right)$$

$$T(s) = \frac{\phi_{out}(s)}{\phi_{in}} = \frac{I_p}{2\pi}\left(R_p + \frac{1}{sC_p}\right)\frac{k_{VCO}}{s}$$

$$= \frac{I_p k_{VCO}(R_p C_p s + 1)}{2\pi C_p s^2}$$





Closed loop frequency response

Bandwidth

$$\omega_h = \omega_{3dB} = \omega_n \left[1 + 2\zeta^2 + \sqrt{2\zeta^2 + 1)^2 + 1} \right]^{1/2}$$

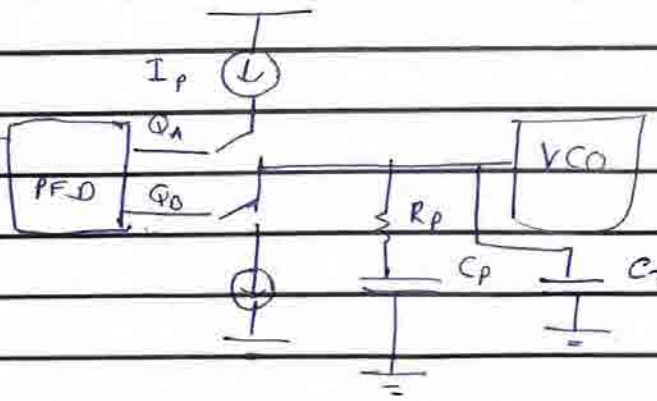
$\omega_{3dB} = 2\omega_n$ for $\zeta = 0.707$

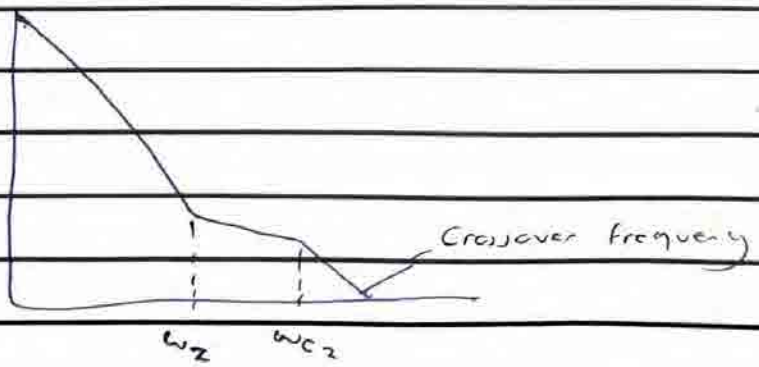
$\omega_{3dB} = 2.5\omega_n$ for $\zeta = 1$

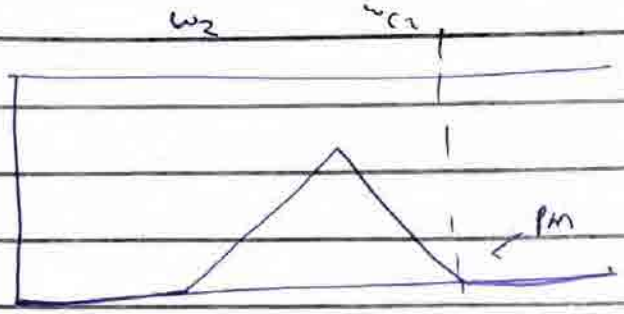
Third-order CP PLL

The Third-order CP PLL counteracts the pulse of variable width the P.D produces that activate the switches to either charge or discharge the capacitor C_p it is fixed by adding a second capacitor C_2 ; it filters out the jump response of the series RC network.

C_2 adds a third pole of finite frequency that will reduce the stability of the PLL $\omega_{C_2} = \dfrac{C_p + C_2}{R_p C_p C_2}$







PLL phase noise

for frequency synthesis, considering low phase noise

- reference noise - usually small since we frequently use a crystal oscillator
- VCO noise - often high
  - phase noise filtering by the PLL

Reference noise

$$\frac{\phi_{out}}{\phi_{ref}} = \frac{\text{Forward path}}{1 + T(s)} = \frac{\frac{K_v \frac{F(s)}{s}}{1 + \frac{K_v F(s)}{Ns}}}{}$$

$$= \frac{N\left(1 + \frac{s}{\omega_2}\right)}{\frac{Ns^2}{K_v} + \frac{s}{\omega_2} + 1}$$

low pass transfer function its magnitude approaches N as s becomes small

$$\frac{\phi_{out}}{\phi_{ref}} = N$$

VCO noise

$$\frac{\phi_{out}}{\phi_{VCO}} = \frac{\text{Forward path}}{1 + T(s)} = \frac{1}{1 + \frac{K_v F(s)}{Ns}}$$

$$= \frac{Ns^2/K_v}{\frac{Ns^2}{K_v} + \frac{s}{\omega_2} + 1}$$

high pass closed loop transfer function. It approaches a magnitude of 1 as s becomes large

while LC VCOs can have low phase noise, they have smaller tuning range. RC or ring oscillator VCOs can be built with very wide tuning range but poor phase noise. PLL can be used to clean up the VCO phase noise with the loop bandwidth