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Course: Analog IC Design and Applications - EEE 524

Analog Multipliers

Introduction

Nonlinear operations on continuous-valued analog signals are often required in instrumentation, communication, and control system design. Analysis of commonly used techniques for performing multiplication and division within a monolithic integrated circuit is done in this chapter.

The Emitter-Coupled pair as a single multiplier

The emitter-coupled pair, is shown to produce output currents that were related to the differential input voltage by: $I_{c1} = \frac{I_{EE}}{1+\exp(-V_{id}/V_T)}$ $I_{c2} = \frac{I_{EE}}{1+\exp(V_{id}/V_T)}$

$$\Delta I_c = I_{c1} - I_{c2} = I_{EE} \tanh(V_{id}/2V_T)$$

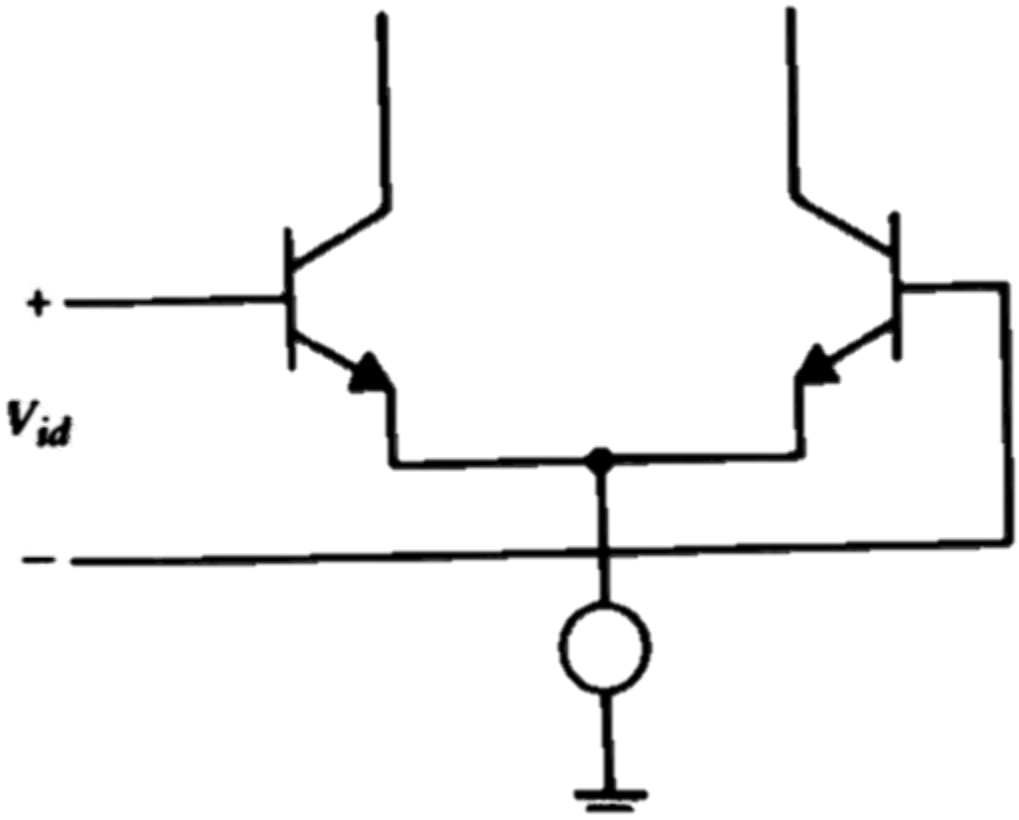


Figure 1: Emitter-Coupled pair circuit

Gilbert multiplier cell

The restriction to two quadrants of operation is a severe one for many communications applications, and most practical multipliers allow four-quadrant operation. The Gilbert multiplier cell is a modification of the emitter-coupled cell, which allows four-quadrant multiplication.

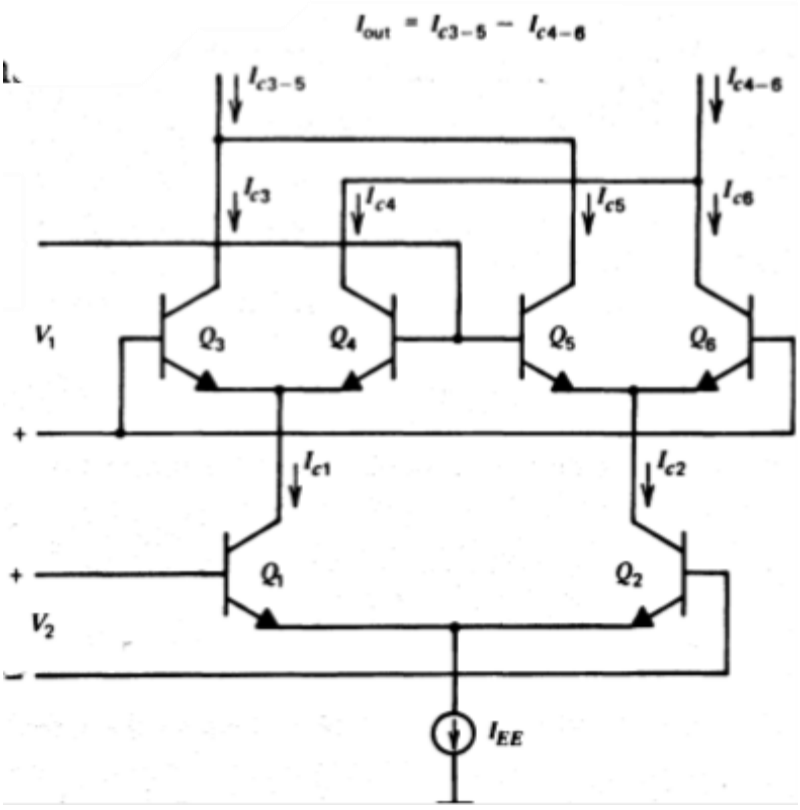


Figure 2: Gilbert multiplier cell

$$I_{c3} = \frac{I_{c1}}{1 + \exp(-V_{id}/V_{T)}}$$

$$I_{c4} = \frac{I_{c1}}{1 + \exp(V_{id}/V_{T)}}$$

$$I_{c5} = \frac{I_{c2}}{1 + \exp(V_{id}/V_{T)}}$$

$$I_{c6} = \frac{I_{c2}}{1 + \exp(-V_{id}/V_{T)}}$$

$$\Delta I = I_{c3-5} - I_{c4-6} = I_{c3} + I_{c5}(I_{c4} + I_{c6}) = (I_{c3} - I_{c6}) - (I_{c4} - I_{c5})$$
$$= I_{EE} \tanh(V_1/2V_T) \tanh(V_2/2V_T)$$

Gilbert cell Applications

- Multiplier – Gilbert cell can be used for analog multiplication of small-amplitude signals.
- Pre-warping circuit inverse hyperbolic tangent -

$$\Delta V = 2V_T \tanh^{-1}\left(\frac{K_1 V_1}{I_{o1}}\right)$$

$$\Delta I = I_{EE}\left(\frac{K_1 V_1}{I_{o1}}\right)\left(\frac{K_2 V_2}{I_{o2}}\right)$$

- Complete Analog Multiplier- $V_{out} = I_{EE} K_3 \frac{K_1}{I_{o1}} \frac{K_2}{I_{o2}} V_1 V_2 = 0.1 V_1 V_2$
- Balanced Modulator- In communications systems, the need frequently arises for the multiplication of a continuously varying signal by a square wave. This is easily accomplished with the multiplier circuit by applying a sufficiently large signal directly to the cross-coupled pair.
- Phase detector - If unmodulated signals of identical frequency coo are applied to the two inputs, the circuit behaves as a phase detector and produces an output whose dc component is proportional to the phase difference between the two inputs.

PHASE LOCKED LOOPS

A PLL is a feedback system that includes a VCO, phase detector, and low pass filter within its loop. Its purpose is to force the VCO to replicate and track the frequency and phase at the input when in lock. The PLL is a control system allowing one oscillator to track with another. It is possible to have a phase offset between input and output, but when locked, the frequencies must exactly track.

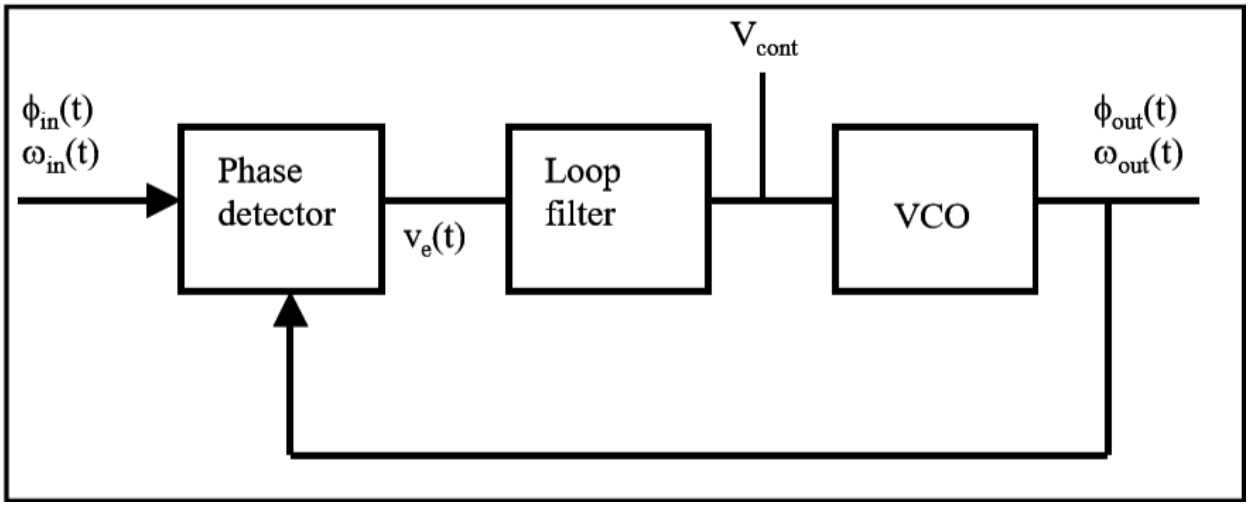


Figure 3: Phase Locked Loop Block diagram

Phase detector:

Phase detector compares the phase at each input and generates an error signal, $V_e(t)$, proportional to the phase difference between the two inputs. KD is the gain of the phase detector (V/rad).

$$V_e(t) = K_D[\emptyset_{out}(t) - \emptyset_{in}(t)]$$

$$V_e(t) = A(t)B(t)$$

$$A(t) = A\cos(\omega_0 t + \emptyset_A)$$

$$B(t) = B\cos(\omega_0 t + \emptyset_B)$$

Since the two inputs are at the same frequency when the loop is locked, we have one output at twice the input frequency and an output proportional to the cosine of the phase difference. The low-pass loop filter must remove the doubled frequency component. Any phase difference then shows up as the control voltage to the VCO, a DC or slowly varying AC signal after filtering.

PLL dynamic response:

To see how the PLL works, suppose that we introduce a phase step at the input at t = t1.

$$\emptyset_{in} = \omega_1 t + \emptyset_0 + \emptyset_1 u(t - t_1)$$

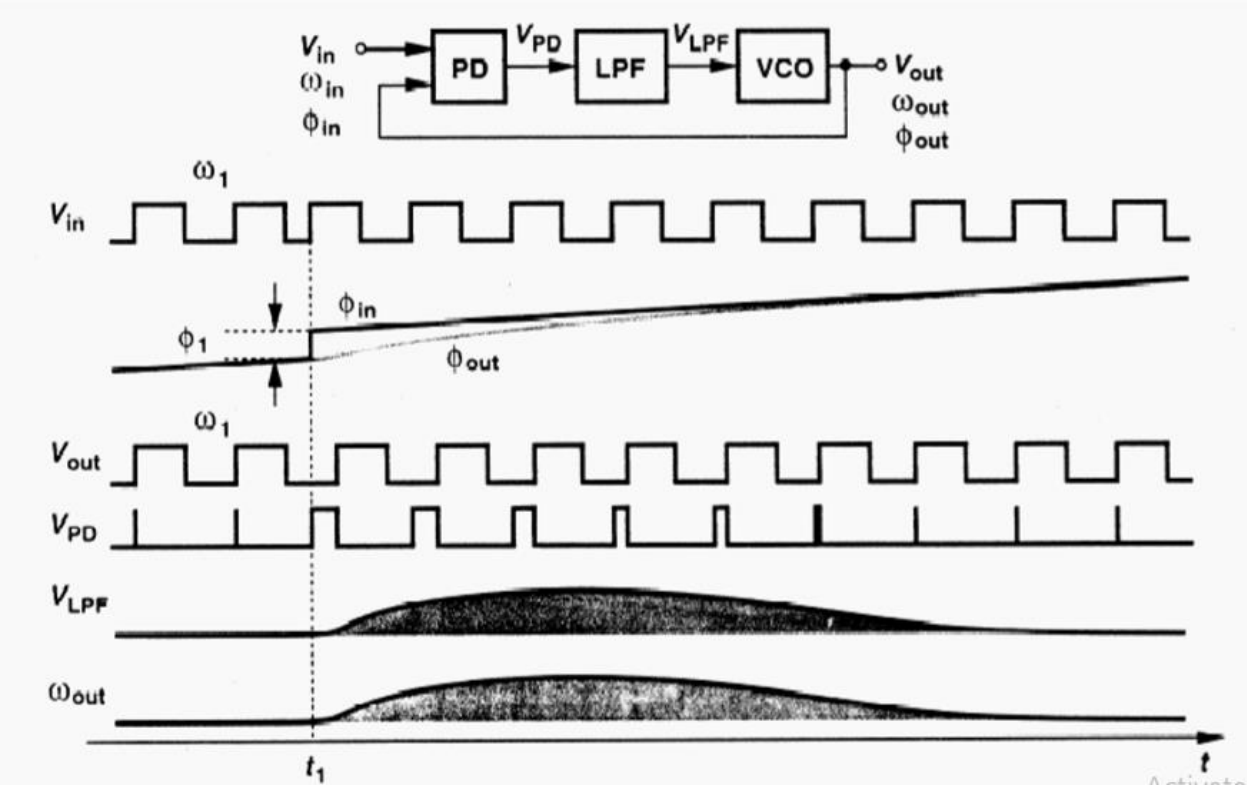


Figure 4: PLL dynamic response

Lock Range:

Range of input signal frequencies over which the loop remains locked once it has captured the input signal. This can be limited either by the phase detector or by the VCO frequency range.

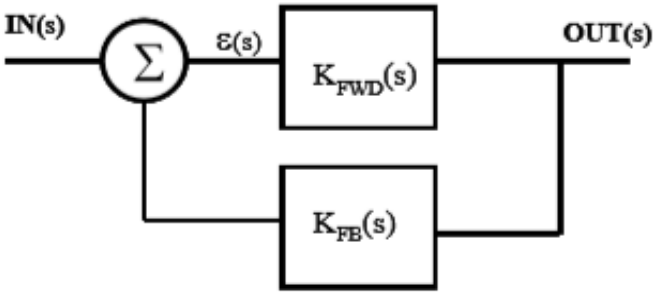
Capture Range:

Range of input frequencies around the VCO center frequency onto which the loop will lock when starting from an unlocked condition. Sometimes a frequency detector is added to the phase detector to assist in initial acquisition of lock.

Approach:

The PLL is treated as a linear feedback system and it is assumed that it is already locked to the reference signal, a frequency domain approach is used.

PLL is a feedback system



Loop Gain: $T(s) = K_{FWD}(s)\,K_{FB}(s)$

Transfer Function: $\dfrac{OUT(s)}{IN(s)} = H(s) = \dfrac{K_{FWD}(s)}{1 + T(s)}$

The Loop gain can be described as a polynomial:

$$T(s) = \frac{K'(s+a)(s+b)\cdots}{s^n\,(s+\alpha)(s+\beta)\cdots}$$

ORDER = the order of the polynomial in the denominator

TYPE = n (the exponent of the s factor in the denominator)

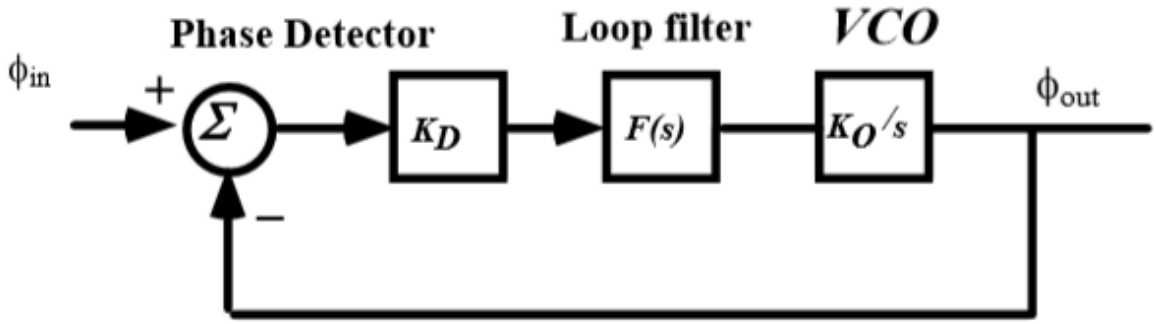
PHASE ERROR = $\varepsilon(s) = \dfrac{IN(s)}{1 + T(s)}$

STEADY STATE ERROR = $\varepsilon_{SS} = \lim_{s \to 0}[s\varepsilon(s)] = \lim_{t \to \infty} \varepsilon(t)$

(this is the Laplace Transform final value theorem)

Frequency and Phase Tracking loop:

A PLL with a feedback of 1 is considered and the frequencies of the input and output are identical hence the input and output can track each other.



Transfer Function: H(s) = forward path gain / [1 + T(s)].

With feedback = 1,

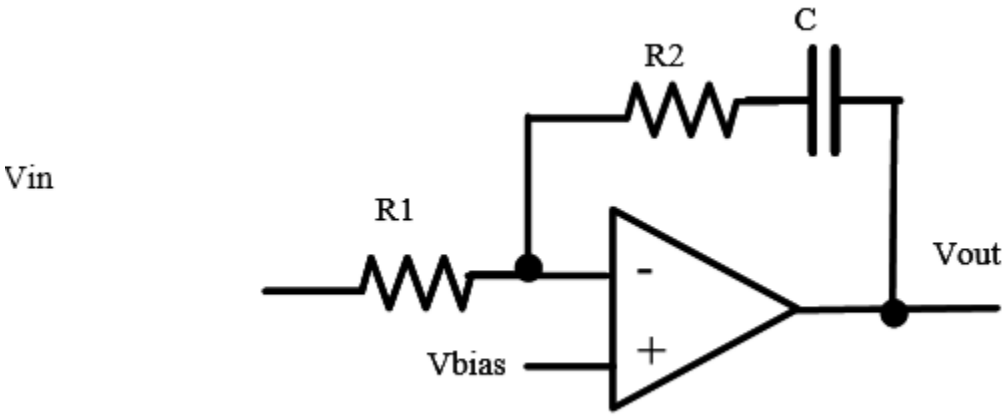
$$H(s) = T(s)/[1 + T(s)]$$

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{K_D K_O F(s)/s}{1 + K_D K_O F(s)/s}$$

Phase error function:

$$\varepsilon_s = \phi_{in} - \phi_{out} = \frac{s\phi_{in}}{s + K_D K_O F(s)}$$

Loop filter OP-AMP:

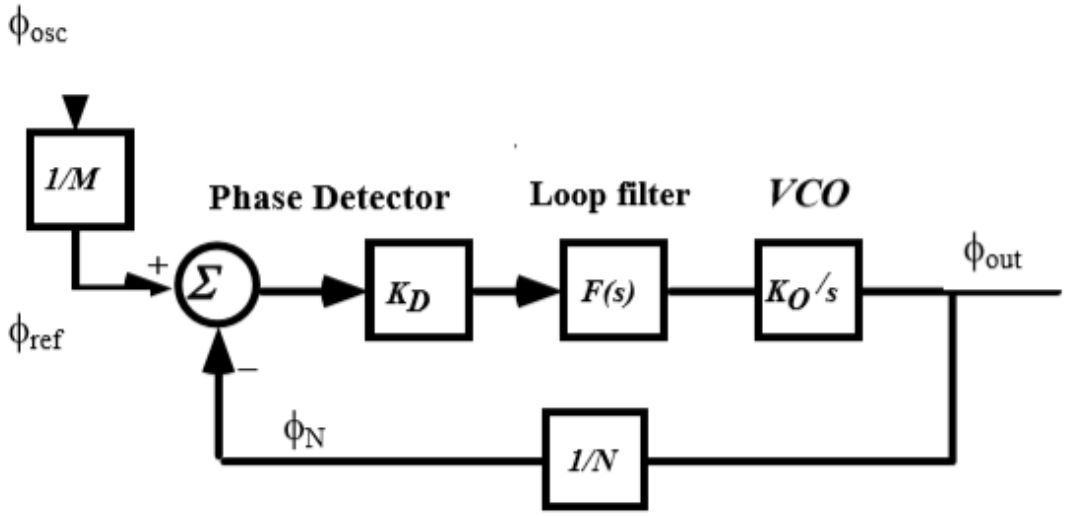


An op amp can be used to form a filter that includes a pole at s = 0 and a finite zero. For example, the circuit above can be analyzed using the virtual ground approximation to obtain F(s).

$$F(s) = \frac{V_{out}}{V_{in}} = \frac{1 + sR_2C}{sR_1C}$$

Synthesizer PLL:

A divider 1/N to the feedback path. This architecture is called an "integer-N" synthesizer.



Thus,

$$\frac{\phi_N}{\phi_{out}} = \frac{1}{N}$$

and also, $N = \frac{\omega_{out}}{\omega_{ref}}$

We can calculate the loop gain, T(s):

$$T(s) = \frac{K_D K_O F(s)}{Ns}$$

- We see that the loop gain is reduced by a factor of N.
- Also, in most applications, N is not constant, so
- KV = KDKO is not a constant – varies with frequency according to the choice of N

$$F(s) = \frac{1 + s/\omega_2}{s/\omega_1}$$

Phase Frequency Detector:

The phase-frequency detector is a widely used architecture in frequency synthesizers. As opposed to the XOR phase detector, this one produces two outputs: QA and QB, or as is customary, UP and DOWN respectively.

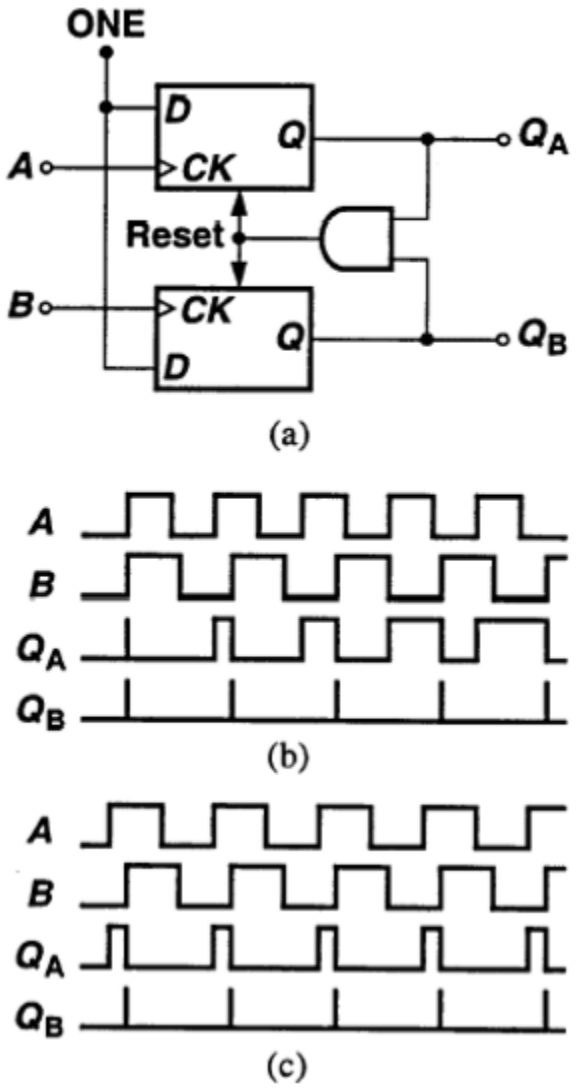


Figure 5: (a) phase/frequency detector (b) response (c) response

Charge pump loop filter:

An alternative loop filter implementation called the charge pump is widely used for many applications. It is very convenient to implement in CMOS.

• The PFD output produces UP (QA) and DOWN (QB) pulses whose width is proportional to the phase error.

• Charge pump current sources I1 and I2 must produce exactly equal currents. They charge and discharge the capacitor, CP, in discrete steps.

• If there is a static phase error Δϕ at the PFD input, the capacitor, C, will be charged indefinitely – therefore, the DC gain is infinite: an ideal integrator. So, we expect to have zero static phase error. This is unlike the type I loop which gave Δϕ = Δω/KV steady state phase error.

• The CP PLL will detect small phase errors and correct them as long as the frequency of the phase error (jitter frequency) is within the loop 3 dB bandwidth. This phase comparison occurs on every cycle.

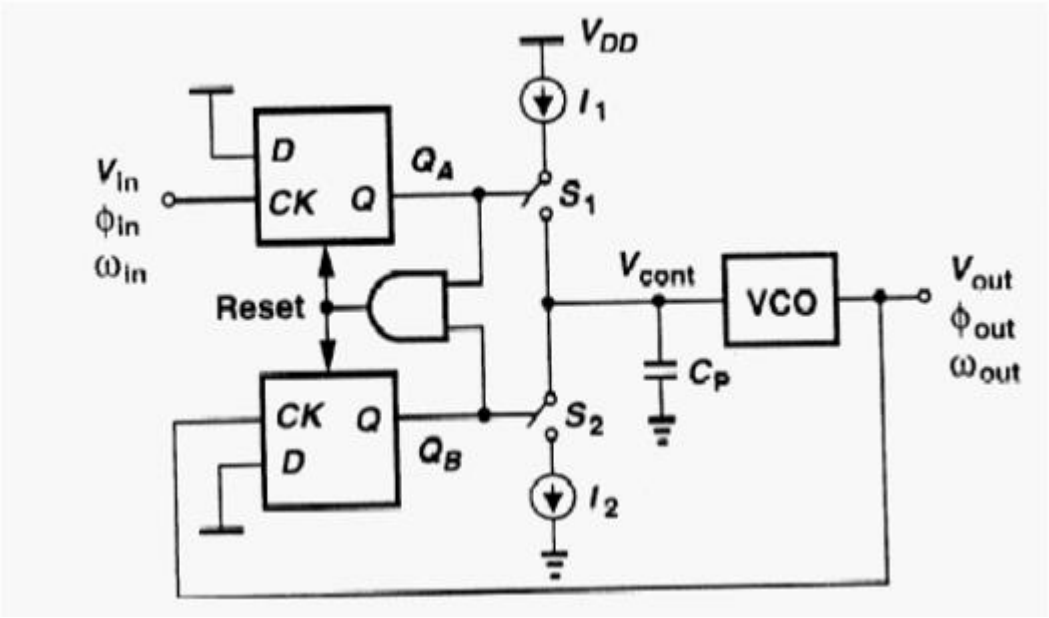
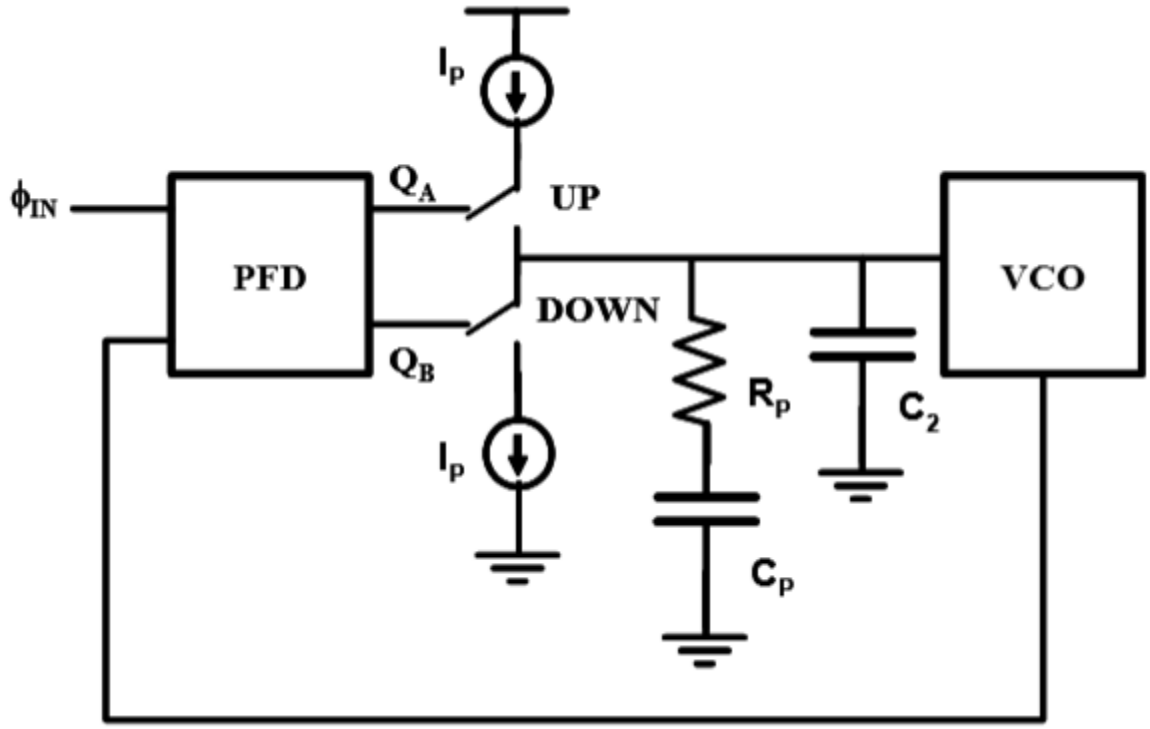


Figure 6: simple charge pump PLL

Third order CP-PLL:

One residual problem is overlooked. The phase detector produces pulses of variable width that activate the switches to either charge or discharge the capacitor CP. Now that a resistor has been added, however, we find that the control voltage coming out of the charge pump will jump up or down before settling to its steady state value. This occurs because the voltage across a capacitor cannot be instantaneously changed, so the initial voltage drop occurs across RP, which then charges CP exponentially. This jumpy control voltage frequency modulates the VCO at the reference frequency, creating reference spurs. This is not such a big problem if N = 1 because the jump will be at the same frequency as the VCO. But, at larger N values, it creates sidebands and jitter.

So, we need to fix this by adding a second capacitor, C2, whose function is to filter out the jumpy response of the series RC network. The magnitude of the reference spur sidebands is reduced by a factor of ωREF/ωC2. Unfortunately, however, C2 adds a third pole of finite frequency that will reduce the stability of the PLL.



PLL Phase Noise:

We have considered how the bandwidth of the loop affects things like settling time and capture range. But it also plays a role in the PLL noise behavior.

For frequency synthesis, we are interested in low phase noise. There are at least 2 main sources:

1. reference noise – usually small since we frequently use a crystal oscillator

2. VCO noise – often high. We hope that the PLL will suppress most of the noise, at least close to the carrier.

The effect caused by each of these noise sources can be seen from the closed loop transfer functions.

Reference noise

$$\frac{\emptyset_{out}}{\emptyset_{ref}} = \frac{Forward\ path}{1+T(s)} = \frac{K_v F(s)/s}{1+K_v F(s)/Ns} = \frac{N(1+\frac{s}{\omega_2})}{\frac{Ns^2}{K_v}+\frac{s}{\omega^2+1}}$$

VCO noise

$$\frac{\emptyset_{out}}{\emptyset_{vco}} = \frac{Forward\ path}{1+T(s)} = \frac{1}{1+K_v F(s)/Ns} = \frac{Ns^2/K_v}{\frac{Ns^2}{K_v}+\frac{s}{\omega^2+1}}$$

Conclusions:

1. Reference input noise (reference source noise, data jitter, phase noise on FM input signal, etc.) sees a low-pass transfer function. It is passed through and multiplied by N. All we can do is try to avoid making it worse with our loop. A narrow bandwidth loop filter will help to suppress high frequency noise coming into the PLL from the reference port.

2. VCO jitter is suppressed by the PLL within the loop bandwidth. It has a high-pass transfer function. Thus, to suppress VCO noise, we want a large loop bandwidth.

Reference spurs:

The Integer N PLL has an inherent conflict between the frequency step size (increment) and the settling time/bandwidth. The phase detector produces pulses that are at the reference frequency, f_R. These pulses are filtered by the loop low pass filter, but not completely. Any residual reference frequency component on the VCO tuning voltage produces frequency modulation. Sidebands called reference spurs appear on both sides of the desired output spectral line spaced by f_R.

The natural frequency of the loop must be well below the reference frequency so that the reference frequency component is well attenuated by the loop filter.

$$\omega_n \leq \omega_R/10$$

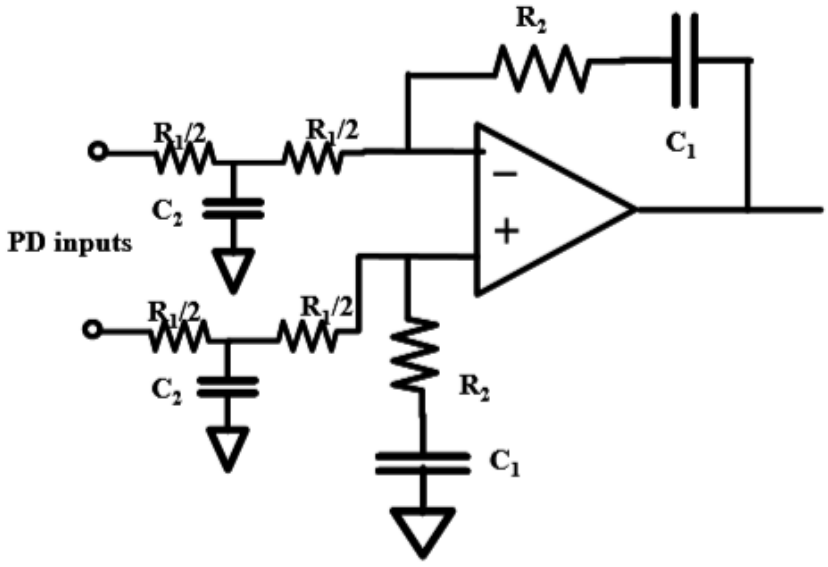


Figure 7: Third order loop