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EEE524 Phase Lock Loop

A PLL is a feed back system that Includes a VCO, Phase detector and low pass filter within it's loop; the purpose is to force the VCO to replicate and track the frequency and phase at the Input when in lock.

Loop Gain: $T(s) = K\ FWD(s) \cdot K_{FB}(s)$ out(s)

$H(s) = K\ FWD(s)$

PLL is a Feed back System

Transfer Function: $\Sigma$ (KFWD(s) · $K_{FB}(s)$ |N(s)| 1 + T(s)

$K_{FB}(s) \cdot T(s) = K(s+a)(s+b)$ sn $(s+a)(s+B)$

order = the order of the polynomial in the denominator.

The loop gain can be described as a polynomial.

Steady State Error $= E_{SS} = \lim_{t \to \infty} [sE(s)] = \lim_{s \to 0} E(t)$

(This is the laplace transform final value theorem)

SS is a Characteristic of feed back Control System

From the Gardner's book illustrates how the phase Error, Expressed as $E(s) = 20 \log (\Phi_{out} / \Phi_{in})$ dB Increases as the Input Frequency approaches the Natural loop Frequency For the Case with $\zeta = 0.707$ For Input Phase Variations well below the loop bandwidth, the loop tracks Very well

Phase Error: There is no Frequency Error when the loop is locked.

Input Frequency = output frequency. But, it is Impossible to have a phase Error For Some Input transient Phase Conditions.

if the loop frequency is lower than the Cross over frequency is lower than the Cross over frequency. which

which you might want to do to attenuate the high frequency ripple from the phase detector, then the phase margin can become unacceptably small.

if $A(t) = A\cos(\omega_0 t + \phi_A)$

$B(t) = B\cos(\omega_0 t + \phi_B)$, Then, $A(t), B(t) =$

$(AB/2)\{\cos(2\omega t + \phi_A + \phi_B) + \cos(\phi_A - \phi_B)$

Since two Inputs are at the same frequency when the loop is locked, we have one output at twice the Input frequency and an output proportional to the Cosine of the phase difference.

$\phi_{in}(t)$ $\omega_{in}(t)$ $\phi_{out}(t)$ $\omega_{out}(t)$ Phase and frequency are Interrelated by: $\omega(t) = d\phi/dt$ $\phi(t) = \phi(0) + \int \omega(t')$

Applications:

There are many applications for the PLL, but we will study

a) when Integrated by the loop filter, this causes the Control Voltage of the VCO to move towards the locked Condition of equal frequency and phase.

b) The CPPD PLL will detect small phase errors and Correct them as long as the frequency of the phase error (Jitter Frequency) is within the loop 3dB bandwidth. The phase frequency detector (PFD) with single capacitor Cp has $H(s) = V_{out}(s) = I_p = K_{PFD}\Delta\phi$

2nd Cp's To find the frequency response of the Input Current, we note that, $I(s) = V_{out}(s)/Z(s) = V_{out}(s)/(1/sC_p)$

where $Z(s)$ is the Complex Impedance.

Here we see the phase and frequency step response for a

type 2 PLL in terms of the key loop parameters.

$V_{e-max} = \pm \frac{K_D \pi}{2}$ when the phase detector output voltage

is applied through the loop filter to the VCO,

$\Delta\omega_{out-Max} = \pm \frac{K_V \pi}{2} = \omega_L$.

where $\omega_L$ = Lock range

$K_V = K_O K_D$, the product of the phase detector and VCO gains

Thus loop filter $V_{(O} K_D) \phi_{(N} = 1 \phi_{out N}$

and also, $N = \omega_{out} / \omega_{ref}$, ~~Phase detector $\phi$ $\phi_{out}$~~

We can calculate the loop gain $T(s)$: $T(s) = K_D K_O F(s) \cdot \frac{1}{N_s}$

We see that the loop gain is reduced by a factor of N

with feedback = 1,

phase detector $\phi_{ref}$ in $F(s)$

Phase error function: $H(s) = T(s) / [1 + T(s)]$

~~$H(s) = \phi_{out} / K_V K_O F(s) \frac{1}{s}$~~

For the frequency application, we want to have ideally perfect phase tracking for phase and frequency steps.

The phase error needed to generate the control voltage steps varies inversely with the loop gain.

Also in most applications, N is not constant, so

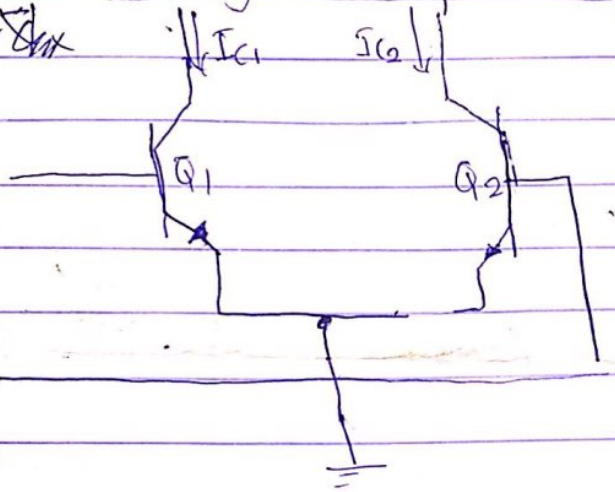
$K_V = K_D K_O$ is not a constant, it varies with frequency according to the choice of N using the $F(s)$ determined for the op amp.

pole-zero loop filter: $F(s) = \frac{1 + s/\omega_2}{s/\omega_1}$

# ANALOG MULTIPLIERS

Non linear operations on continuous Valued analog systems are often required in Instrumentation, Communication and Control design. These operations Include

- Rectification, modulation, demodulation, Multiplication and division
- In analog processing the need often arises for a circuit that takes two analog Inputs and produces an output proportional to their product. Such Circuits are termed as Analog multipliers




$$I_{C1} = \frac{I_{EE}}{1+\exp(-V_{id}/V_T)} \qquad I_{C2} = \frac{I_{EE}}{1+\exp(V_{id}/V_T)}$$

The Current $I_{EE}$ is the bias Current for the Emitter Coupled pair. $I_{EE}$ is proportional to the Input Signal. Thus we have

$$I_{EE} = K_0 (V_{12} - V_{BE(on)})$$

The Gilbert multiplier Cell is the basis for most Integrated balanced Multiplier Systems. The Series Connection of an Emitter-Coupled pair with two Cross-Coupled, Emitter-Coupled pairs. Produces a particular useful transfer Characteristic

Gilbert cell applications:

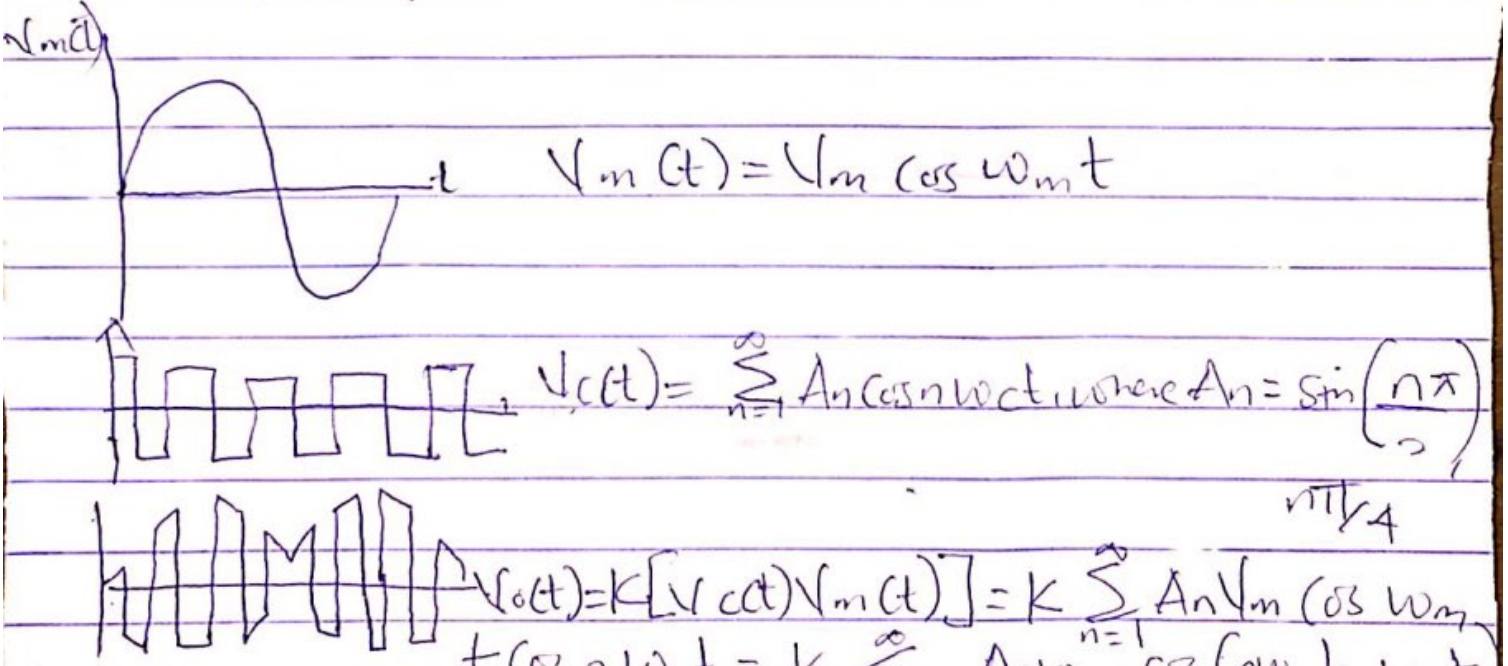
1) If $V_1 < V_T$ and $V_2 < V_T$ Then $\tanh(V_{1,2}/2V_T) = V_{1,2}/2$ and it works as a Multiplier.
2) if one of the Inputs of a signal that is large Compared

by a square wave, and acts as a Modulator.

3.) if both Inputs are large Compared to $V_T$, and all six transistors in the Circuit behave as nonsaturating switches. This is useful for the detection of phase differences between two amplitude limited signals, as is required in PLL

## Gilbert Cell as a balanced modulator

In Communication Systems, the need frequently arises for the multiplication of a Continuously Varying signal by a square wave. This is easily accomplished with the multiplier Circuit by applying a sufficiently large signal directly to the Cross Coupled pair




## Gilbert as a phase detector

- If unmodulated signals of identical frequency $\omega_0$ are applied to the two Inputs, the Circuits behave as a phase detector and produces an output whose dc Component is proportional to the phase diff btw the two Inputs

The dc Comp is given by $V_{avg} = \frac{1}{2\pi} \int_0^{2\pi} V_o(t)\, d(\omega_0 t) = \frac{1}{\pi}[A_1 - A_2$