Note Summary.

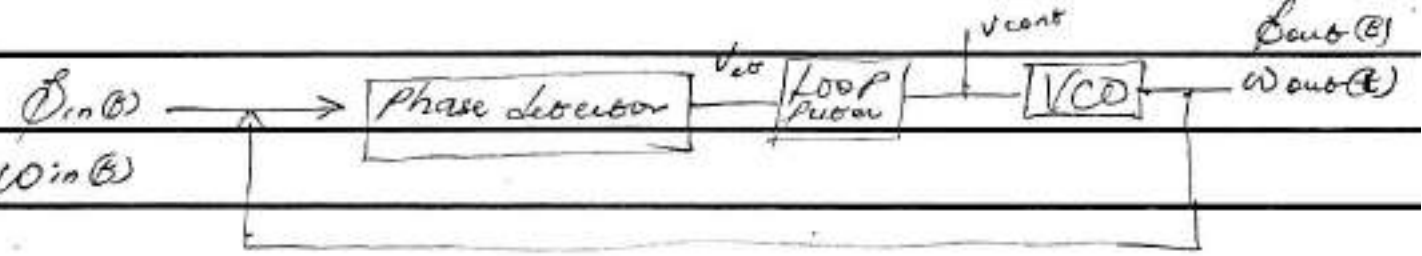
- A PLL is a feedback system that contains a VCO (Voltage Controlled Oscillator), Phase detector & a low pass filter, thus making it a closed loop system
- The function of the PLL circuit is to mimic and then track the frequency ($\omega_{in}(t)$) & phase ($\phi_{in}(t)$) when in lock mode

Mathematically,

$$\phi_{out}(t) - \phi_{in}(t) + const \quad \text{---} (1)$$

$$\frac{d}{dt}\omega_{out}(t) - \omega_{in}(t) \quad \text{---} 2$$

In eqn 2 Frequency between inputs are identical
in eqn 1 Phase offset is possible between inputs.



When output is taken from the V_{cont} terminal, a baseband output is produced that traces the variations in phase at the input.

When output is taken from the VCO, it acts as an oscillator to generate clock signals that digital systems e.g. microprocessors can utilize to function.

Note the relationship between Phase ϕ & frequency is given as

$$\omega(t) = \frac{d\phi}{dt}$$

where ϕ = phase
ω = frequency.

$$\phi(t) = \phi(0) + \int_0^t \omega(t')\,dt'$$

PLL finds application in

(i) Clock generators (as mentioned earlier)

(ii) Frequency Synthesizers

(iii) Clock Recovery in Serial Datalink.

Phase Detector: It compares the phase at the two inputs, and generates an error signal based on the difference between the two ($V_e(t)$). The phase detector has a gain of K_d

$$V_e(t) = K_d(\phi_{out}(t) - \phi_{in}(t))$$

* The phase locked loop tracks the phase of input signals.
* The phase detector is an example of an analog multiplier.
* Error signal is proportional to phase error.
* The loop filter is a low pass filter.
* Its transfer function is characterized by $F(s) = \frac{1 + s/\omega_2}{1 + s/\omega_1}$
* The LPF suppresses noise & unwanted phase detector outputs.

VCO

* The VCO is a linear time invariant system
* The VCO frequency is characterized by its input voltage.

Recall an analog multiplier takes the product of 2 signals. $V_e(t) = A(t)B(t)$ so

$\therefore$ If $A(t) = A\cos(\omega_0 t + \phi_A)$

$B(t) = B\cos(\omega_0 t + \phi_B)$

$$\cos\alpha\cos\beta = \frac{\cos(\alpha+\beta) + \cos(\alpha-\beta)}{2}$$

Let $(\omega_0 t + \phi_A) = \alpha$

$\phi\ (\omega_0 t + \phi_B) = \beta$

$$\Rightarrow AB \times \frac{\cos((\omega_0 t + \phi_A) + (\omega_0 t + \phi_B)) + \cos((\omega_0 t + \phi_A) - (\omega_0 t + \phi_B))}{2}$$

$$\Rightarrow A(B(t)) \Rightarrow (AB/2)[\cos(2\omega_0 t + \phi_A + \phi_B) + \cos(\phi_A - \phi_B)]$$

∴ Because the two inputs are at the same frequency when the loop is locked, we have one output term at the input frequency ($2\omega_0 t$), and an output proportional to the cosine of the phase difference ($\cos(\phi_A - \phi_B)$).

After this stage the double frequency component is passed through an ~~BPF~~ LPLF.

* Any phase difference is sensed as control voltage to the VCO or a DC or slowly varying AC.

Vco - linear, time invariant system.

* Excess phase of the VCO is the system output.

$$\phi_{out} = K_{vco} \int_{-\infty}^{t} V_{cont}\, dt'$$

The frequency is assumed to be linearly proportional to the control voltage.

$$\omega_{out} = \omega_0 + K_0 V_{cont}$$

PLL dynamic response

If a phase step is introduced

$$\phi_{in} = \omega_1 t + \phi_0 + \phi_{14}(t - t_1)$$

(6) causes the final & initial frequencies to be the same

5) Lock Range: Range of input over which the input remain locked after the input signal has been captured.

* Phase detector or the VCO freq. range

6) Capture range: Range of input frequencies around the VCO center freq. on which the loop will lock when starting from an unlocked position.