NAME: OBILOM CHIDERA 16/ENG04/068

EEE 524 ASSIGNMENT

SUMMARY OF THE NOTE GIVEN TO US

Digital Modulation is the process of using discrete signals to modulate a carrier wave. ASK, FSK, PSK, and QAM are all forms of digital modulation.

ANALOG SHIFT KEYING (ASK)

If the information signal is digital and the amplitude (lV of the carrier is varied proportional to the information signal, a digitally modulated signal called amplitude shift keying (ASK) is produced.

Mathematically, amplitude-shift keying is;

$$v_{(ask)}(t) = [1 + v_m(t)]\left[\frac{A}{2}\cos(\omega_c t)\right]$$

Where;

- Vask(t) = amplitude-shift keying wave
- Vm(t) = digital information (modulating) signal (volts)
- A/2 = unmodulated carrier amplitude (volts)
- wct = analog carrier radian frequency (radians per second, 2fct)

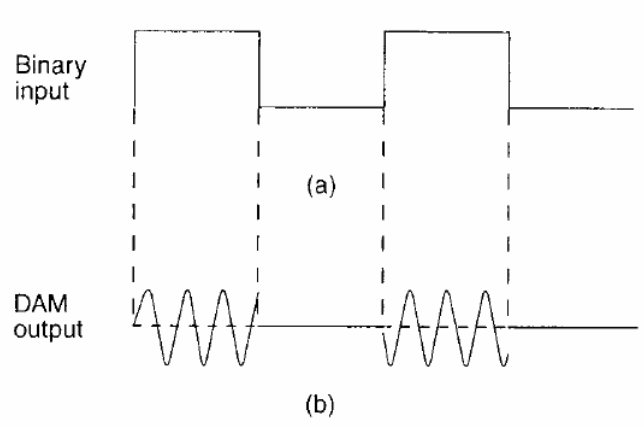


Figure 1: ASK Modulated signal

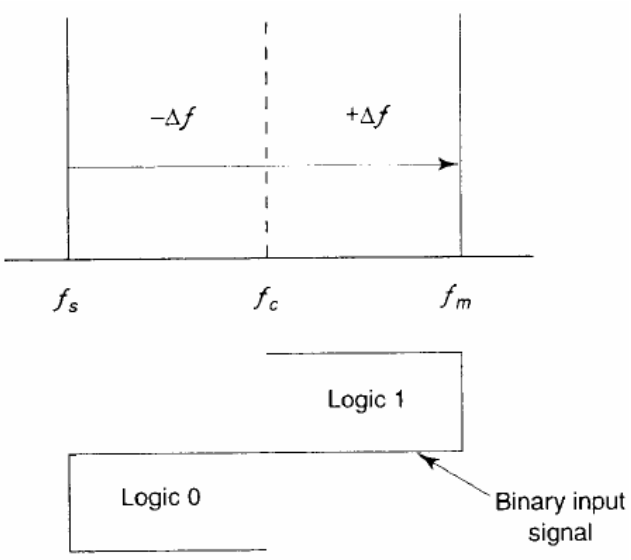
FREQUENCY SHIFT KEYING (FSK)

If the frequency (f) is varied proportional to the information signal, frequency shift keying (FSK) is produced. The general expression for FSK is;

$$v_{fsk}(t) = V_c \cos\{2\pi[f_c + v_m(t)\,\Delta f]t\}$$

Where;

- Vfsk(t) = binary FSK waveform
- Vc = peak analog carrier amplitude (volts)
- fc = analog carrier center frequency (hertz)
- Δf = peak change (shift) in the analog carrier frequency (hertz)
- vm(t) = binary input (modulating) signal (volts)



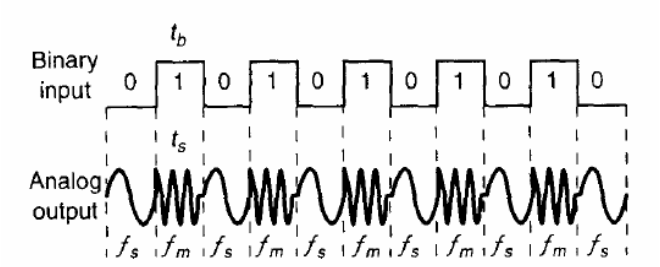


Figure 2: FSK Modulated Signal

Where;

- fm = mark frequency
- fs = space frequency
- fc = carrier frequency
- tb = time of one bit
- ts = time of space bit

Baud for binary FSK = 2(Δf+fb)

Noncoherent FSK demodulator

The FSK input signal is simultaneously applied to the inputs of both bandpass filters (BPFs) through a power splitter. The respective filter passes only the mark or only the space frequency on to its respective envelope detector. The envelope detectors, in turn, indicate the total power in each passband, and the comparator responds to the largest of the two powers. This type of FSK detection is referred to as noncoherent detection.

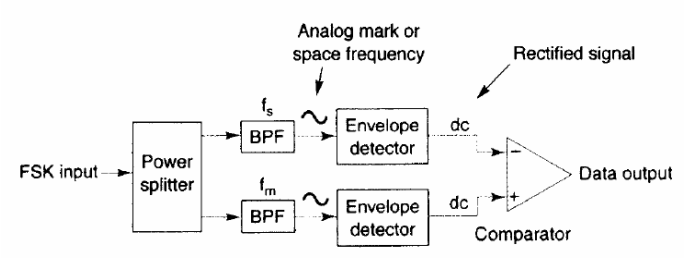


Figure 3: Block Diagram of Noncoherent FSK Demodulator

Coherent FSK receiver

The incoming FSK signal is multiplied by a recovered carrier signal that has the exact same frequency and phase as the transmitter reference. However, the two transmitted frequencies (the mark and space frequencies) are not generally continuous; it is not practical to reproduce a local reference that is coherent with both of them. Consequently, coherent FSK detection is seldom used.

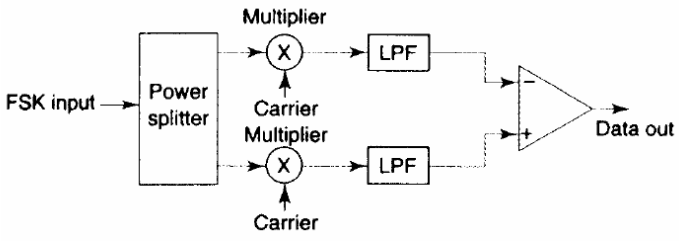


Figure 4: Block Driageam of Coherent FSK Receiver

PHASE-SHIFT KEYING (PSK)

If the phase of the carrier (0) is varied proportional to the information signal, phase shift keying (PSK) is produced.

The simplest form of PSK is **binary phase-shift keying (BPSK)**, where N = 1 and M = 2. Therefore, with BPSK, two phases (21 = 2) are possible for the carrier. One phase represents a logic 1, and the other phase represents a logic 0. As the input digital signal changes state (i.e., from a 1 to a 0 or from a 0 to a 1), the phase of the output carrier shifts between two angles that are separated by 180°.

Quaternary Phase-Shift Keying (QPSK)

Quaternary Phase-Shift Keying QPSK is an M-ary encoding scheme where N = 2 and M= 4 (hence, the name "quaternary" meaning "4"). A QPSK modulator is a binary (base 2) signal, to produce four different input combinations,: 00, 01, 10, and 11. Therefore, with QPSK, the binary input data are combined into groups of two bits, called dibits. In the modulator, each dibit code generates one of the four possible output phases (+45°, +135°, -45°, and -135°).

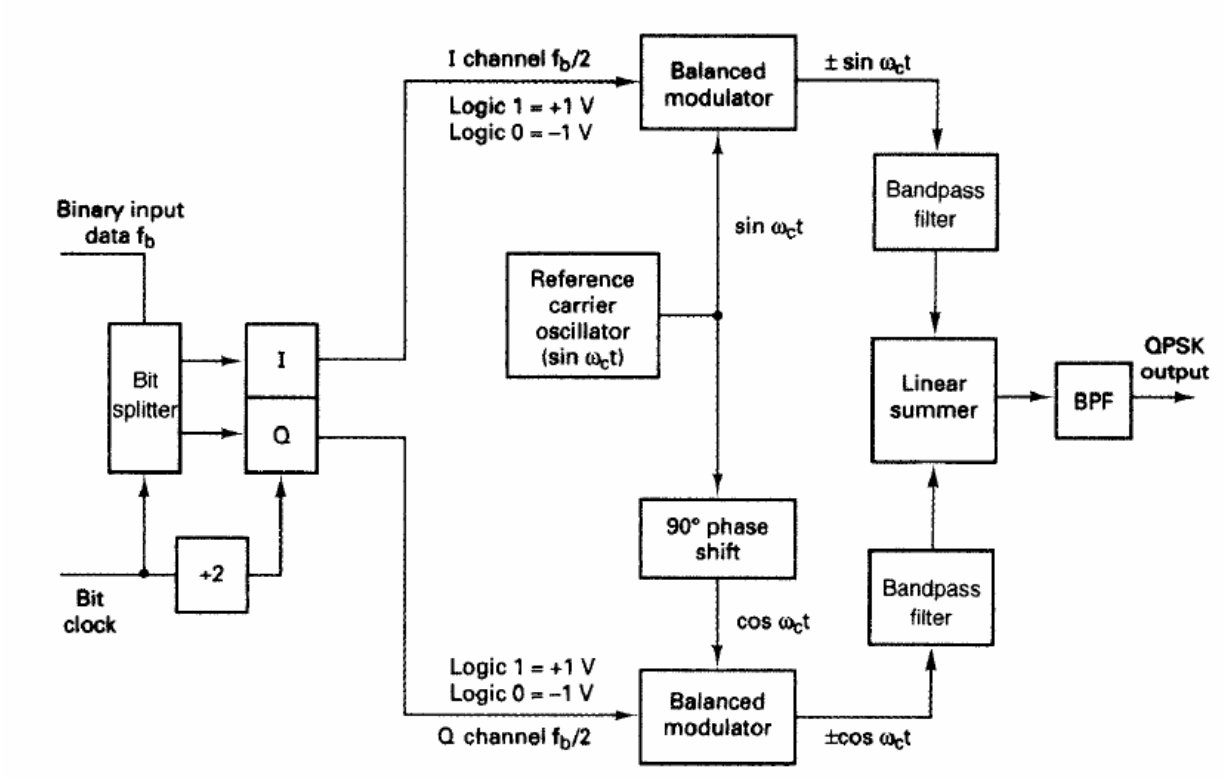


Figure 5: Block Diagram of QPSK

8-PSK

With 8-PSK, three bits are encoded, forming tribits and producing eight different output phases. To encode eight different phases, the incoming bits are encoded in groups of three, called tribits (23 = 8).

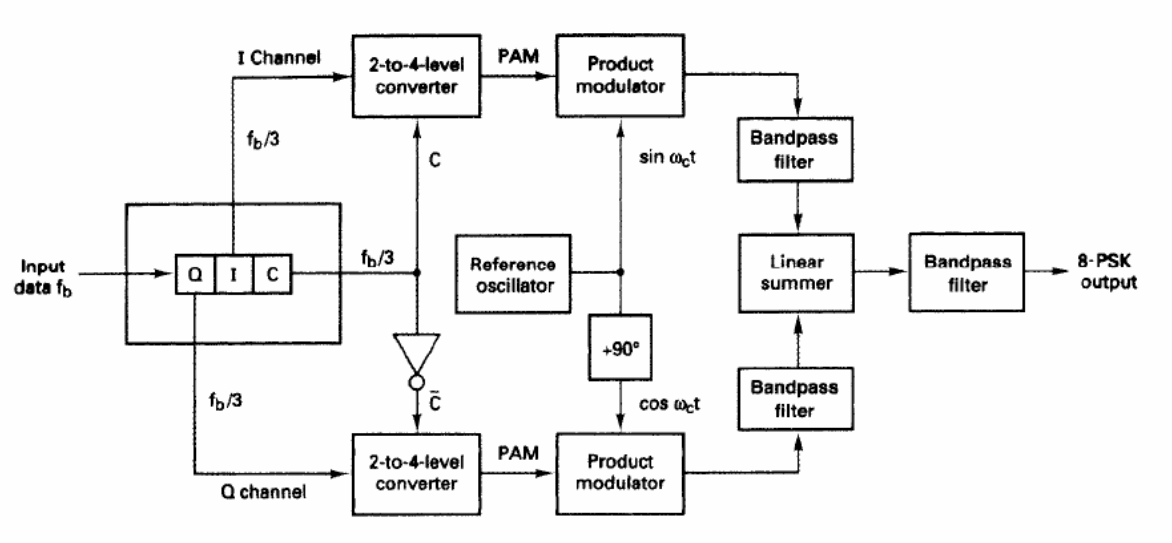


Figure 6:Block Diagram of 8-PSK

Bandwidth considerations of 8-PSK.

With 8-PSK, because the data are divided into three channels, the bit rate in the I, Q, or C channel is equal to one-third of the binary input data rate (fb /3).

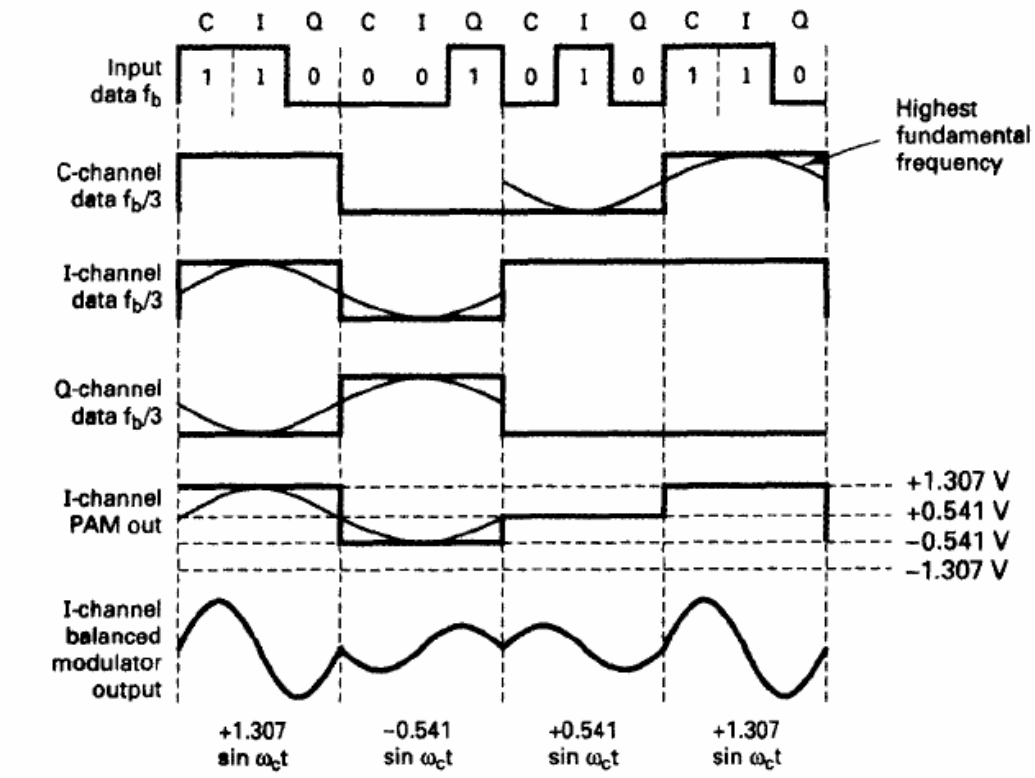


Figure 7: Wave Diagram for 8-PSK

16-PSK

16-PSK is an M-ary encoding technique where M = 16; there are 16 different output phases possible. With 16-PSK, four bits (called quadbits) are combined, producing 16 different output phases. With 16-PSK, n = 4 and M = 16; therefore, the minimum bandwidth and baud equal one-fourth the bit rate (fb/4).

QUADRATURE – AMPLITUDE MODULATION (QAM)

If both the amplitude and the phase are varied proportional to the information signal, quadrature amplitude modulation (QAM) results.

8-QAM

8-QAM is an M-ary encoding technique where M = 8. Unlike 8- PSK, the output signal from an 8-QAM modulator is not a constant-amplitude signal.

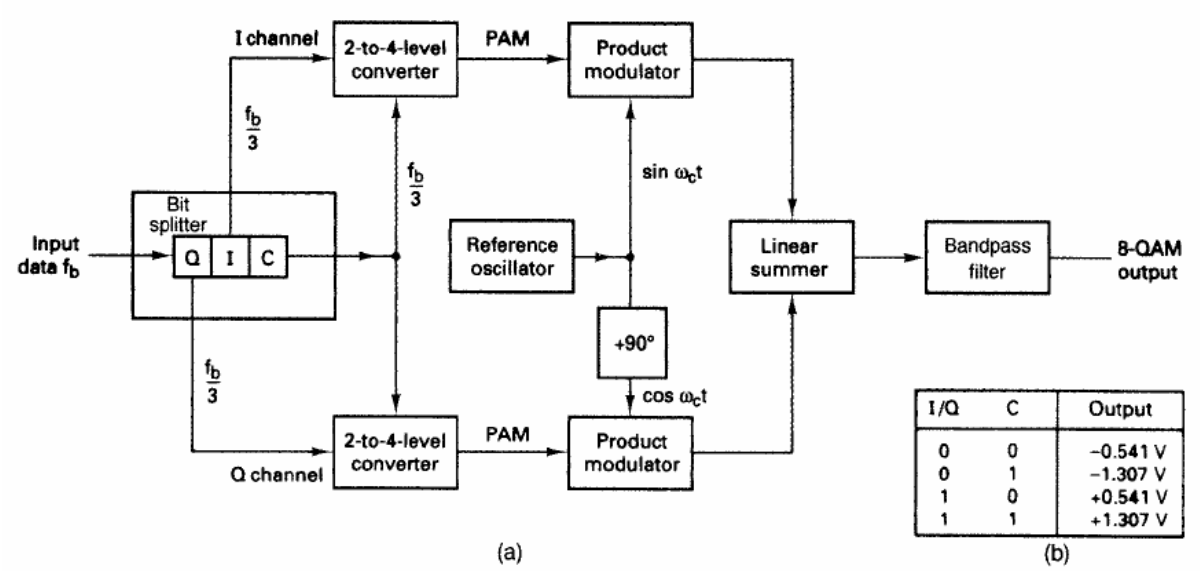


Figure 8: Block Diagram for 8-QAM transmitter

The minimum bandwidth required for 8-QAM is fb / 3, the same as in 8-PSK.

An 8-QAM receiver is almost identical to the 8-PSK receiver shown in Figure 2-28.

16-QAM

As with the 16-PSK, 16-QAM is an M-ary system where M = 16. The input data are acted on in groups of four (24 = 16). As with 8-QAM, both the phase and the amplitude of the transmit carrier are varied.

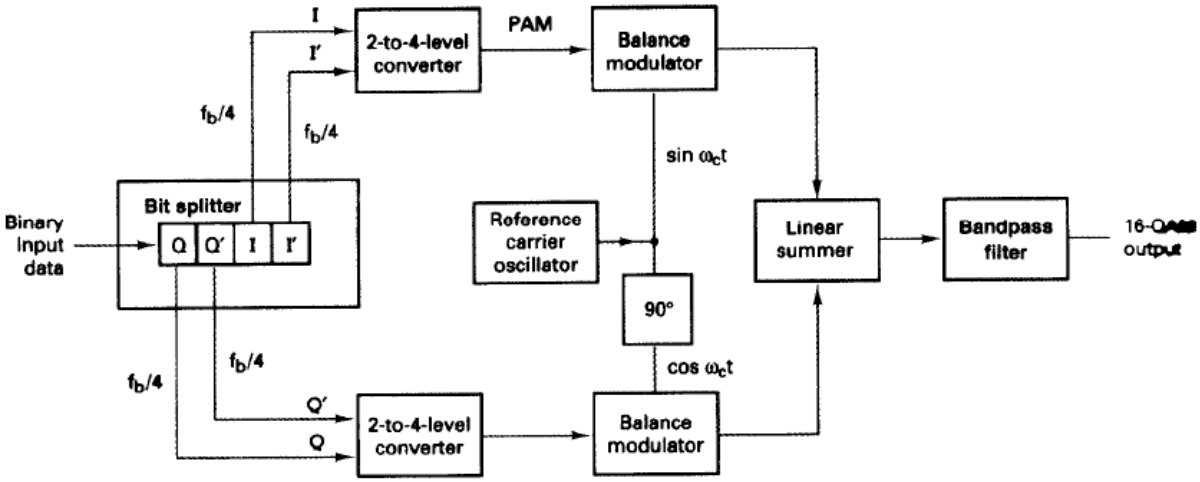


Figure 9:Block Diagram for 16-QAM

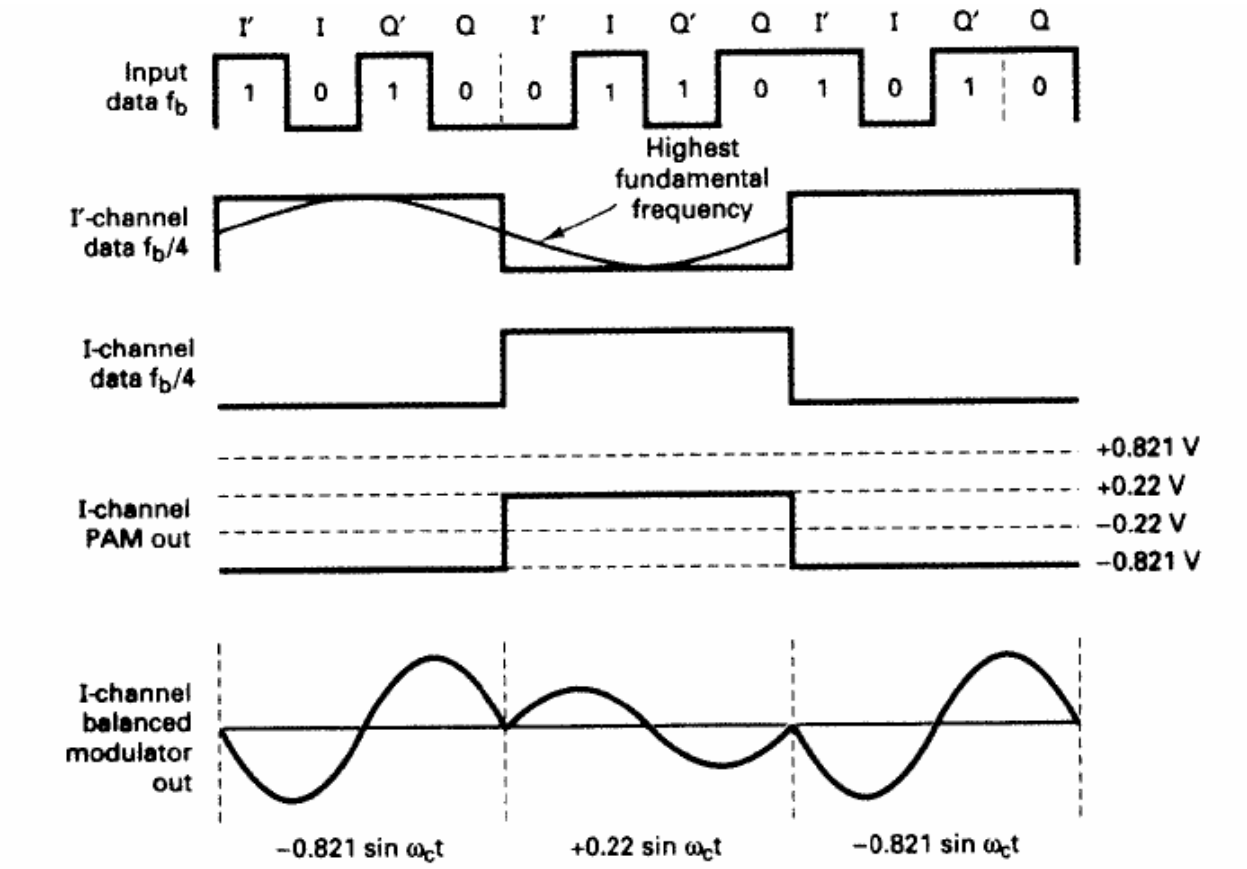


Figure 10: Phase Diagram for 16-QAM

BANDWIDTH EFFICIENCY

Bandwidth efficiency (sometimes called information density or spectral efficiency, often used to compare the performance of one digital modulation technique to another. Mathematical bandwidth efficiency is;

$$B\eta = \frac{transmission\ bit\ rate\ (bps)}{\min imum\ bandwidth\ (Hz)} = \frac{bits/s}{Hertz}$$

Where Bη = bandwidth efficiency

DIFFERENTIAL PHASE-SHIFT KEYING

Differential phase-shift keying (DPSK) is an alternative form of digital modulation where the binary input information is contained in the difference between two successive signaling elements rather than the absolute phase.

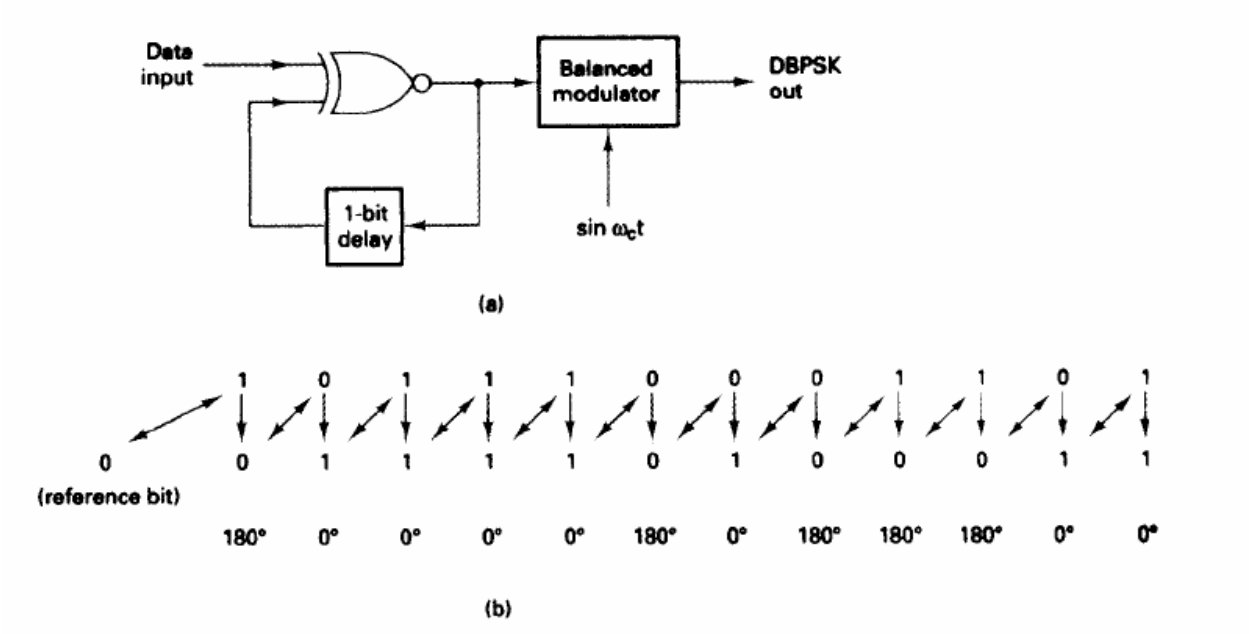


Figure 11: (a) Block Diagram of DPSK Transmitter, (b) Time Diagram of DPSK Transmitter

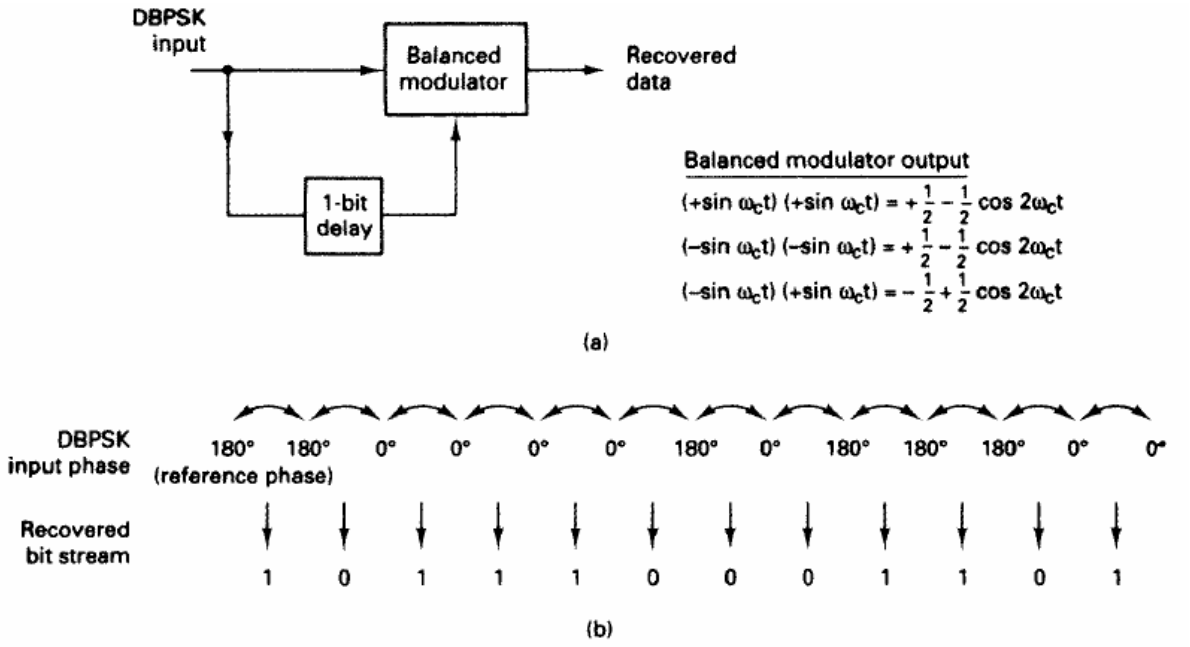


Figure 12: (a) Block Diagram of DPSK Receiver (b) Time Sequence for DPSK Receiver

PROBABILITY OF ERROR AND BIT ERROR RATE

Probability of error P(e) and bit error rate (BER) are often used interchangeably BER is an empirical (historical) record of a system's actual bit error performance.

Carrier-to-noise power ratio is the ratio of the average carrier power (the combined power of the carrier and its associated sidebands) to the *thermal noise power* Carrier power can be stated in watts or dBm. where

$$C_{(dBm)} = 10 \log [C_{(watts)} / 0.001] \quad (2.28)$$

Thermal noise power is expressed mathematically as

$$N = KTB \text{ (watts)} \quad (2.29)$$

where

N = thermal noise power (watts)

K = Boltzmann's proportionality constant ($1.38 X 10^{-23}$ joules per kelvin)

T= temperature (kelvin: 0 K=-273° C, room temperature = 290 K)

B = bandwidth (hertz)

Stated in dBm, $N_{(dBm)} = 10 \log [KTB / 0.001]$ (2.30)

Mathematically, the carrier-to-noise power ratio is

$$C / N = C / KTB \text{ (unitless ratio)} \quad (2.31)$$

where

C = carrier power (watts)

N = noise power (watts)

Stated in dB, $C / N\ (dB) = 10 \log [C / N]$

$$= C_{(dBm)} - N_{(dBm)} \qquad (2.32)$$

Energy per bit is simply the energy of a single bit of information. Mathematically, energy per bit is

$$E_b = CT_b\ (J/bit) \qquad (2.33)$$

where

E_b = energy of a single bit (joules per bit)
T_b = time of a single bit (seconds)
C = carrier power (watts)

Stated in dBJ, $E_{b(dBJ)} = 10 \log E_b \qquad (2.34)$

and because $T_b = 1/f_b$, where f_b is the bit rate in bits per second, E_b can be rewritten as

$$E_b = C / f_b\ (J/bit) \qquad (2.35)$$

Stated in dBJ, $E_{b(dBJ)} = 10 \log C / f_b \qquad (2.36)$

$$= 10 \log C - 10 \log f_b \qquad (2.37)$$

Noise power density is the thermal noise power normalized to a 1-Hz bandwidth (i.e., the noise power present in a 1-Hz bandwidth). Mathematically, noise power density is

$$N_o = N / B\ (W/Hz) \qquad (2.38)$$

where

N_o = noise power density (watts per hertz)
N = thermal noise power (watts)
B = bandwidth (hertz)

Stated in dBm, $N_{o(dBm)} = 10 \log (N/0.001) - 10 \log B$ (2.39)

Combining Equations 2.29 and 2.38 yields

$$N_o = KTB / B = KT \text{ (W/ Hz)} \quad (2.41)$$

Stated in dBm, $N_{o(dBm)} = 10 \log (K/0.001) + 10 \log T$ (2.42)

Energy per bit-to-noise power density ratio is used to compare two or more digital modulation systems that use different transmission rates (bit rates), modulation schemes (FSK, PSK, QAM), or encoding techniques (M-ary).

Mathematically, E_b/N_o is

$$E_b/N_o = (C/f_b) / (N/B) \quad (2.43)$$

where E_b/N_o *is* the energy per bit-to-noise power density ratio. Rearranging Equation 2.43 yields the following expression:

$$E_b/N_o = (C/N) \, x \, (B/f_b) \quad (2.44)$$

where
E_b/N_o = energy per bit-to-noise power density ratio
C/N = carrier-to-noise power ratio
B/f_b = noise bandwidth-to-bit rate ratio

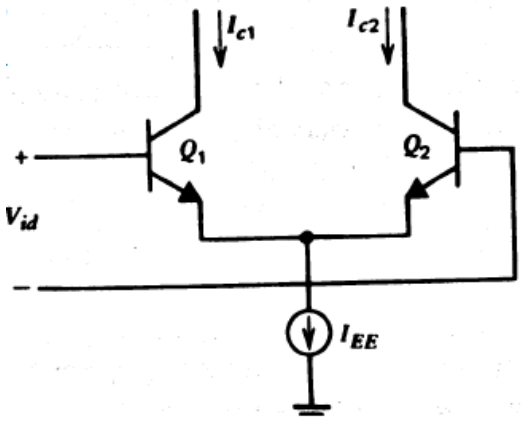
Stated in dB, $E_b/N_o \, (dB) = 10 \log (C/N) + 10 \log (B/f_b)$ (2.45)

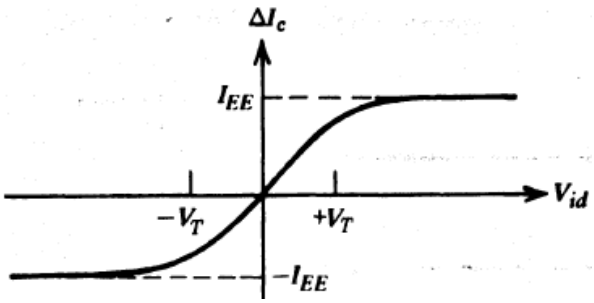
ANALOG MULTIPLIERS

- **The Emitter-Coupled Pair as a Simple Multiplier;**

$$I_{c1} = \frac{I_{EE}}{1+\exp(-V_{id}/V_T)} \quad I_{c2} = \frac{I_{EE}}{1+\exp(V_{id}/V_T)}$$

$$\Delta I_c = I_{c1} - I_{c2} = I_{EE}\tanh(V_{id}/2V_T)$$





- **Gilbert multiplier cell**;

The Gilbert multiplier cell is the basis for most integrated circuit balanced multiplier systems. The series connection of an emitter-coupled pair with two cross-coupled, emittercoupled pairs produces a particularly useful transfer characteristic.

$$I_{c3} = \frac{I_{c1}}{1+\exp(-V_1/V_T)}$$

$$I_{c4} = \frac{I_{c1}}{1+\exp(V_1/V_T)}$$

$$I_{c5} = \frac{I_{c2}}{1+\exp(V_1/V_T)}$$

$$I_{c6} = \frac{I_{c2}}{1+\exp(-V_1/V_T)}$$

Gilbert cell - DC Analysis;

$$I_{c1} = \frac{I_{EE}}{1+\exp(-V_2/V_T)} \quad I_{c2} = \frac{I_{EE}}{1+\exp(V_2/V_T)}$$

- Substituting I_{c1} and I_{c2} in expressions for
- I_{c3} , I_{c4}, I_{c5} and I_{c6} get :

$$I_{c3} = \frac{I_{EE}}{[1+\exp(-V_1/V_T)][1+\exp(-V_2/V_T)]}$$

$$I_{c4} = \frac{I_{EE}}{[1+\exp(V_1/V_T)][1+\exp(-V_2/V_T)]}$$

$$I_{c5} = \frac{I_{EE}}{[1+\exp(V_1/V_T)][1+\exp(V_2/V_T)]}$$

$$I_{c6} = \frac{I_{EE}}{[1+\exp(-V_1/V_T)][1+\exp(V_2/V_T)]}$$

Gilbert cell Applications;

$$\Delta I = I_{c3-5} - I_{c4-6} = I_{c3} + I_{c5} - (I_{c4} + I_{c6}) = (I_{c3} - I_{c6}) - (I_{c4} - I_{c5}) =$$
$$= I_{EE} \tanh(V_1/2V_T) \tanh(V_2/2V_T)$$

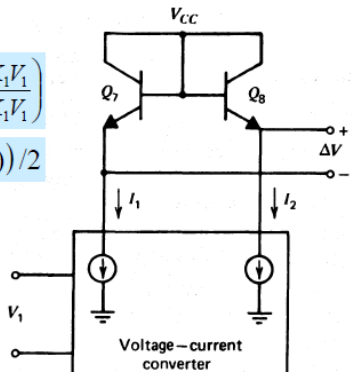
- **Pre-warping circuit - inverse hyperbolic tangent;**

$$I_1 = I_{o1} + K_1 V_1 \text{ and } I_2 = I_{o1} - K_1 V_1$$

- The differential voltage developed across the two diode-connected transistors is

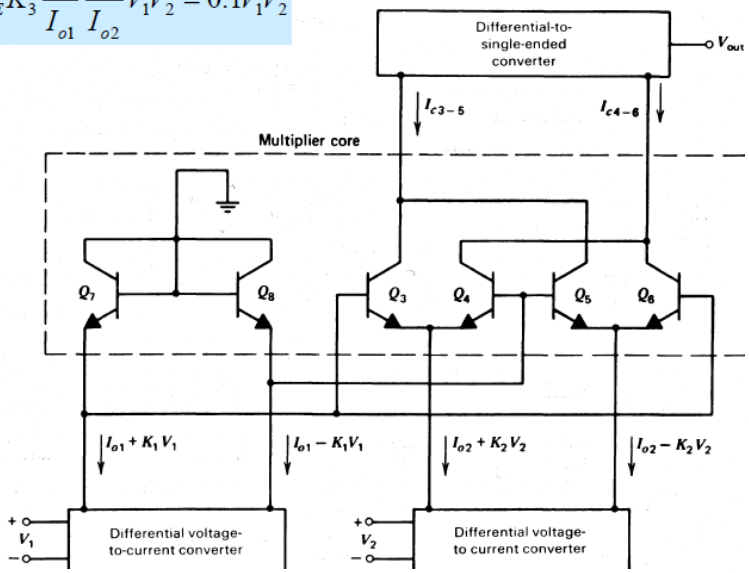
$$\Delta V = V_T \ln\left(\frac{I_{o1}+K_1V_1}{I_s}\right) - V_T \ln\left(\frac{I_{o1}-K_1V_1}{I_s}\right) = V_T \ln\left(\frac{I_{o1}+K_1V_1}{I_{o1}-K_1V_1}\right)$$

- Using the identity: $\tanh^{-1}x = \ln((1+x)/(1-x))/2$
- We get $\Delta V = 2V_T \tanh^{-1}\left(\frac{K_1V_1}{I_{o1}}\right)$
- And finally $\Delta I = I_{EE}\left(\frac{K_1V_1}{I_{o1}}\right)\left(\frac{K_2V_2}{I_{o2}}\right)$



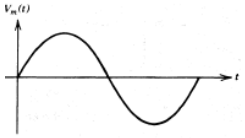
- **Complete Analog Multiplier;**

$$V_{out} = I_{EE} K_3 \frac{K_1}{I_{o1}} \frac{K_2}{I_{o2}} V_1 V_2 = 0.1 V_1 V_2$$

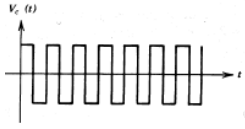


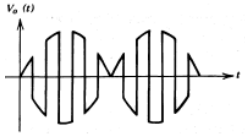
- **Gilbert cell as a Balanced Modulator;**

This is easily accomplished with the multiplier circuit by applying a sufficiently large signal directly to the cross-coupled pair.



Large – signal modulating input





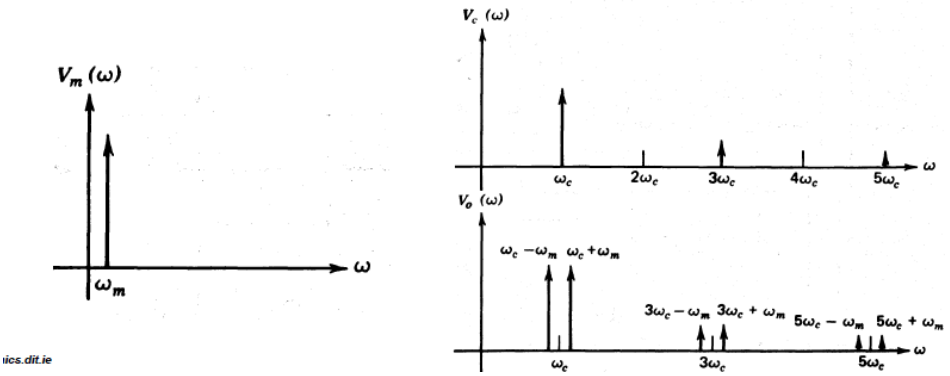
nics.dit.ie

$$V_m(t) = V_m \cos \omega_m t$$

$$V_c(t) = \sum_{n=1}^{\infty} A_n \cos n\omega_c t, \text{ where } A_n = \sin\left(\frac{n\pi}{2}\right) / \frac{n\pi}{4}$$

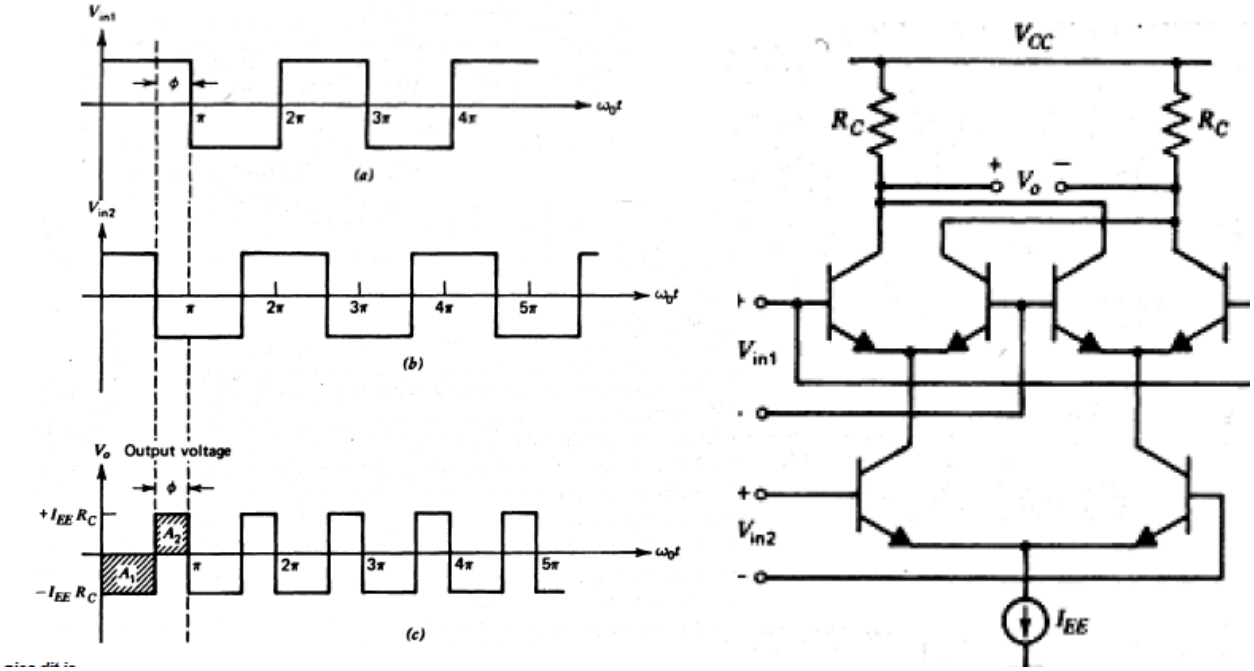
$$V_o(t) = K[V_c(t) V_m(t)] = K \sum_{n=1}^{\infty} A_n V_m \cos \omega_m t \cos n\omega_c t =$$

$$= K \sum_{n=1}^{\infty} \frac{A_n V_m}{2} \cos(n\omega_c t - \omega_n t) \cos(n\omega_c t + \omega_n t)$$



- **Gilbert cell as a phase detector;**

If unmodulated signals of identical frequency coo are applied to the two inputs, the circuit behaves as a phase detector and produces an output whose dc component is proportional to the phase difference between the two inputs.



$$V_{average} = \frac{1}{2\pi}\int_0^{2\pi} V_o(t)\,d(\omega_o t) = \frac{-1}{\pi}[A_1 - A_2]$$

$$V_{average} = -\left[I_{EE}R_C\frac{\pi-\varphi}{\pi} - I_{EE}R_C\frac{\varphi}{\pi}\right] = I_{EE}R_C\left(\frac{2\varphi}{\pi} - 1\right)$$

PHASE LOCKED LOOP (PLL)

A phase-locked loop is a feedback system combining a voltage controlled oscillator (VCO) and a phase comparator so connected that the oscillator maintains a constant phase angle relative to a reference signal. Phase-locked loops can be used, for example, to generate stable output high frequency signals from a fixed low-frequency signal.

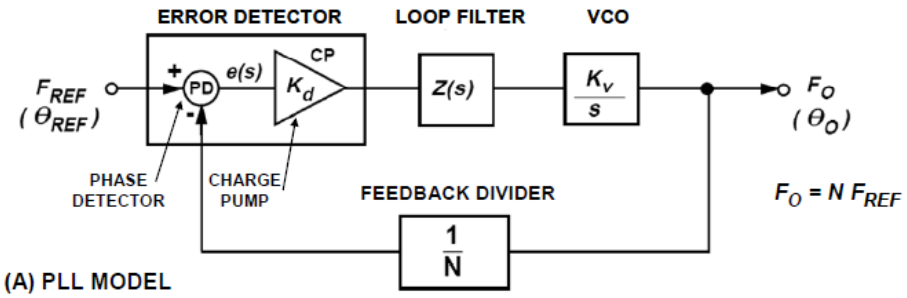


Figure 1: A PLL MODEL

PRESCALERS

In the classical Integer-N synthesizer, the resolution of the output frequency is determined by the reference frequency applied to the phase detector. So, for example, if 200 kHz spacing is required (as in GSM phones), then the reference frequency must be 200 kHz. However, getting a stable 200 kHz frequency source is not easy. A sensible approach is to take a good crystal-based high frequency source and divide it down. For example, the desired frequency spacing could be achieved by starting with a 10 MHz frequency reference and dividing it down by 50.

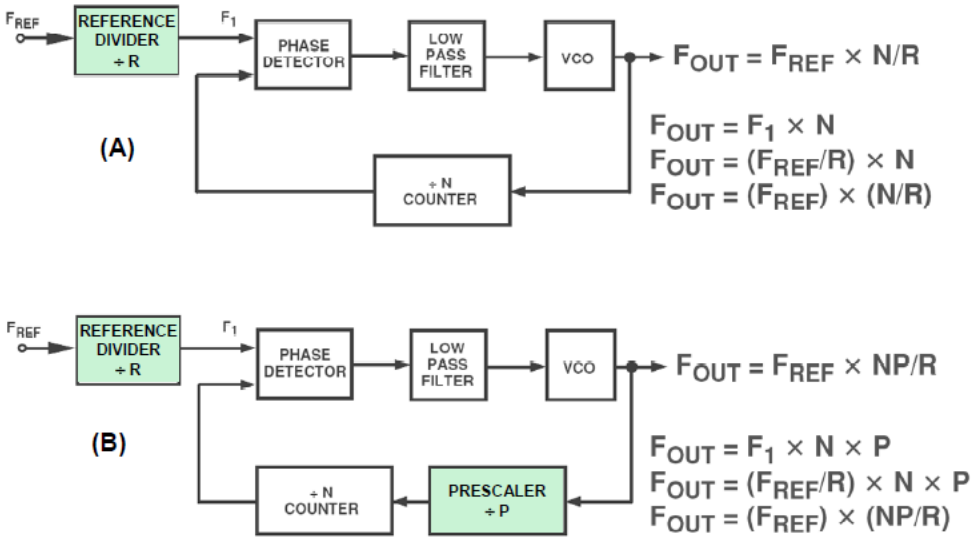


Figure 2: ADDING AN INPUT REFERENCE DIVIDER AND A PRESCALER TO THE BASIC PLL

OSCILLATOR/PLL PHASE NOISE

A PLL is a type of oscillator, and in any oscillator design, frequency stability is of critical importance. We are interested in both long-term and short-term stability. Long-term frequency stability is concerned with how the output signal varies over a long period of time (hours, days, or months). It is usually specified as the ratio, Δf/f for a given period of time, expressed as a percentage or in dB.

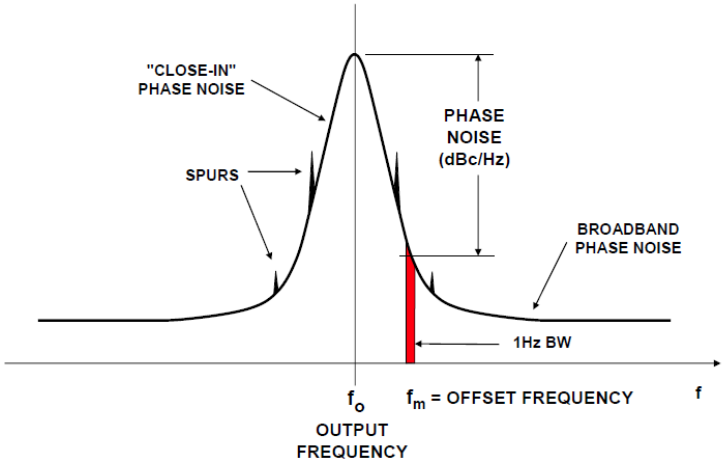


Figure 3: OSCILLATOR PHASE NOISE AND SPURS

FRACTIONAL-N PHASE LOCKED LOOPS

Fractional-N PLLs have been utilized since the 1970s. As has been discussed, the resolution at the output of an integer-N PLL is limited to steps of the PFD input frequency as shown in Figure 7A, where the PFD input is 0.2 MHz.

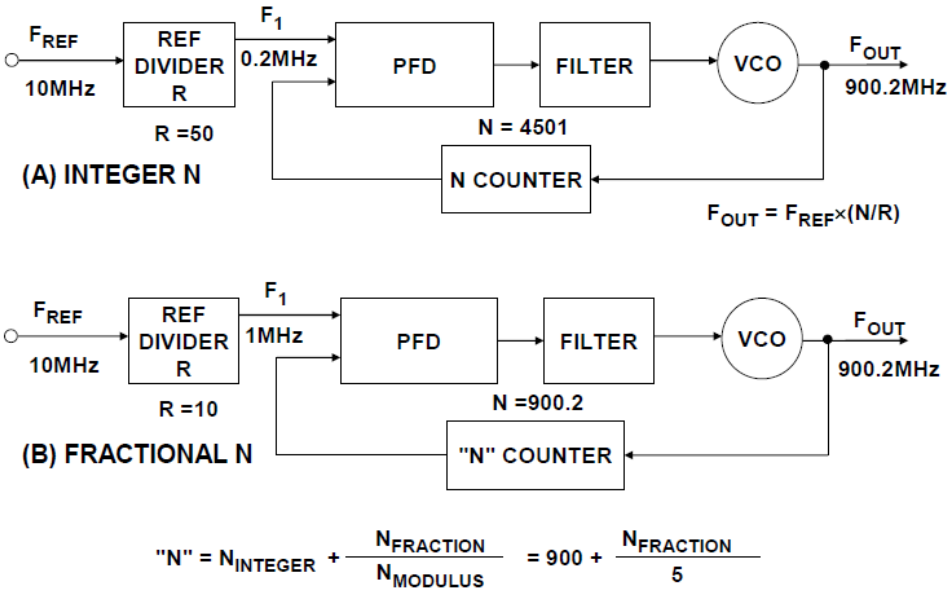


Figure 4: Integer-N Compared to Fractional-N Synthesizer

SIMPLIFYING PLL DESIGN USING ADIsimPLL™

The ADIsimPLL™ software is a complete PLL design package which can be downloaded from the Analog Devices' website. The software has a user-friendly graphical interface, and a complete comprehensive tutorial for first-time users.

The basic design process using ADIsimPLL can be summarized as follows:

1. Choose reference frequency, output frequency range, and channel spacing

2. Select PLL chip from list

3. Select VCO

4. Select loop filter configuration

5. Select loop filter bandwidth and phase margin

6. Run simulation

7. Evaluate time and frequency domain results

8. Optimize