Analog multipliers

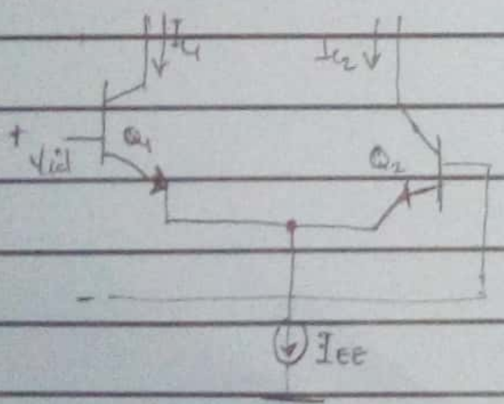
Introduction

* Non-linear operations on continuous-valued analog signals are often required for instrumentation, communication, and control system design. These operations include;

(1) rectification (2) modulation (3) demodulation
(4) Frequency translation (5) multiplication (6) Division.

The most commonly used techniques for performing multiplication and division within a monolithic integrated circuit includes;
(1) The emitter coupled pair as a simple multiplier
(2) Two quadrant restriction
(3) Gilbert multiplier cell
(4) Pre-warping circuit - Inverse hyperbolic tangent.

(1) The emitter coupled-pair as a simple multiplier
The emitter-coupled pair was shown in to produce output currents that were related to the differential input voltage by;

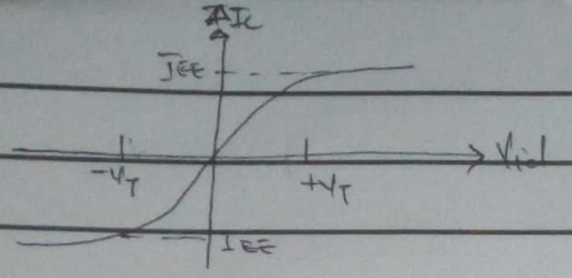


$$I_{c_1} = \frac{I_{EE}}{1 + e^{(-V_{id}/V_T)}}$$

$$I_{c_2} = \frac{I_{EE}}{1 + e^{(V_{id}/V_T)}}$$

$$\Delta I_c = I_{c_1} - I_{c_2}$$
$$= I_{EE} \tanh (V_{id} / 2V_T)$$

The relationship is plotted below and shows that the emitter-coupled pair by itself can be used as a primitive multiplier.



or assuming,

$(V_{id}/2V_T) << 1$, =>

$\Delta I_C = I_{EE}(V_{id}/2V_T)$

where, I_{EE} = Bias current for the emitted coupled pair.

(2) Two quadrant restriction

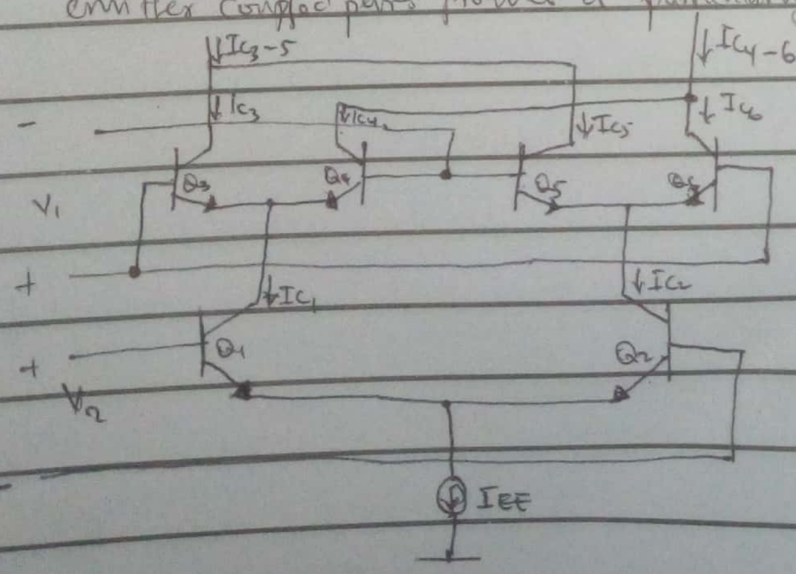
We have produced a circuit that functions as a multiplier under the assumption that V_{id} is small, and that V_{i2} is greater than V_{BE} (on). The latter restriction means that the multiplier functions in only two quadrants of the $V_{id} - V_{i2}$ plane, and this type of circuit is termed a two-quadrant multiplier.

The restrictions to two-quadrant of operation is a severe one for many communications applications and most practical multipliers allow four-quadrant operation.

(3) Gilbert multiplier cell

This is a modification of the emitter-coupled cell, which allows four-quadrant multiplication. Gilbert multiplier cell is the basis for most integrated-circuit balanced multiplier systems.

The series connection of an emitter-coupled pair with two cross-coupled, emitter coupled pairs produces a particularly useful transfer characteristics.



$J_{out} = I_{C3-5} - I_{C4-6}$

$$I_{C3} = \frac{I_{C1}}{1+e^{(-V_1/V_T)}} \qquad I_{C4} = \frac{I_{C1}}{1+e^{(V_1/V_T)}}$$

$$I_{C5} = \frac{I_{C2}}{1+e^{(V_1/V_T)}} \qquad I_{C6} = \frac{I_{C2}}{1+e^{(-V_1/V_T)}}$$

DC - analysis

~~The~~ two currents I_{C1} and I_{C2} are related to th

$$I_{C1} = \frac{I_{EE}}{1+e^{(-V_2/V_T)}} \qquad I_{C2} = \frac{I_{EE}}{1+e^{(V_2/V_T)}}$$

substituting I_{C1} and I_{C2} into I_{C3}, I_{C4}, I_{C5} & I_{C6}

$$I_{C3} = \frac{I_{EE}}{[1+e^{(V_1/V_T)}][1+e^{(-V_2/V_T)}]}$$

$$I_{C4} = \frac{I_{EE}}{[1+e^{(V_1/V_T)}][1+e^{(V_2/V_T)}]}$$

$$I_{C5} = \frac{I_{EE}}{(1+e^{(V_1/V_T)})[1+e^{(V_2/V_T)}]}$$

$$I_{C6} = \frac{I_{EE}}{[1+e^{(-V_1/V_T)}][1+e^{(V_2/V_T)}]}$$

~~Application of Gilbert cell~~

The differential output current is then given by

$$\Delta I = I_{C3-5} - I_{C4-6} = I_{C3} + I_{C5} - (I_{C4} + I_{C6})$$

$$= (I_{C3} - I_{C6}) - (I_{C4} - I_{C5})$$

$$= I_{EE} \tanh(V_1/2V_T) \tanh(V_2/2V_T)$$

The d.c transfer characteristics is the product of the hyperbolic tangent of the two input voltages.

Application of Gilbert cell

The three main application of Gilbert cell depending of the V_1 and V_2 range, include;

(1) If $V_1 < V_T$ and $V_2 < V_T$ then; $\tanh(V_{1,2}/2V_T) \cong V_{1,2}/2V_T$ and it works as multiplier.

(2) If one of the inputs of a signal that is large compared to V_T, this effectively multiplies the applied small signal by a square wave, and acts as a modulator.

(3) If both inputs are large compared to V_T, and all six transistors in the circuit behave as non saturating switches. This is useful for detection of phase differences between two amplitude-limited signals, as is required in phase-locked loops and is sometimes called the phase-detector mode.

Other Uses of Gilbert cell;

(1) Gilbert cell can also be used as a Balanced modulator

(2) Gilbert cell can be used as a phase detector,

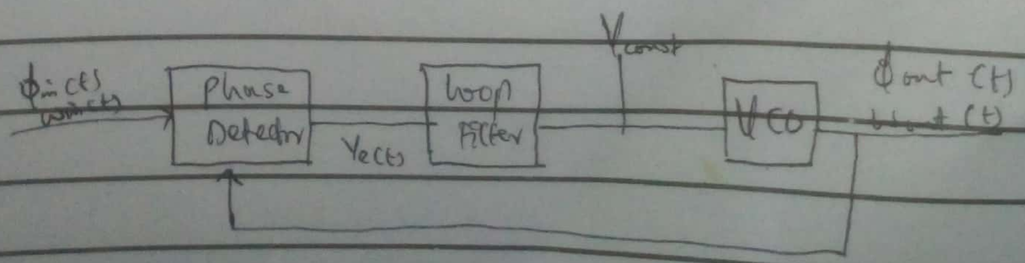
Phase Locked Loop Circuits

Definition

A PLL is a feedback system that includes a VCO, Phase detector and Low pass filter within its loop. Its purpose is to force the VCO to replicate and track the frequency and phase at the input when in lock. The PLL is a control system allowing one oscillator to track with another. It is possible to have a phase offset between input and output, but when locked, the frequencies must exactly track.

$$\phi_{out}(t) = \phi_{in}(t) + Const.$$

$$\omega_{out}(t) = \omega_{in}(t)$$



The VCO output can be used as a local oscillator or to generate a Clock signal for a digital system.

Phase and frequency are interrelated by;

$$\omega(t) = \frac{d\phi}{dt}$$

$$\phi(t) = \phi(0) + \int_0^t \omega(t')\,dt'$$

Applications:

There are many applications for the PLL, but we will study;

a. Clock generation

b. Frequency synthesizer

c. Clock recovery.

(2) phase detector: Compares the phase at each input and generates an error signal $V_e(t)$ proportional to the phase difference between the two inputs, K_D is the gain of the phase detector (V/rad).

$$V_e(t) = K_D \cdot [\phi_{out}(t) - \phi_{in}(t)]$$

Examples; ~~Analog~~ multiplier and mixer.

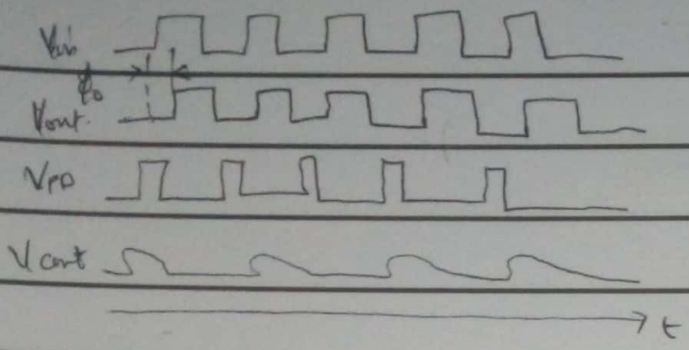
(3) VCO: In PLL applications, the VCO is treated as a linear, time invariant system. Excess phase of the VCO is the system output.

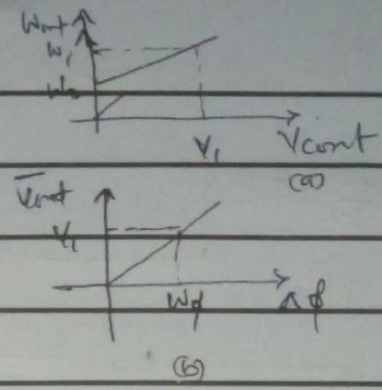
$$\phi_{out} = K_O \int_{-\infty}^{t} V_{cont}\,dt'$$

The VCO oscillates at an angular frequency, W_{out}. It's frequency is set to a nominal W_o when the control voltage is zero.

Frequency is assumed to be linearly proportional to the control voltage with a gain coefficient K_O or K_{VCO} (rad/s/v).

$$W_{out} = W_o + K_O V_{cont}$$

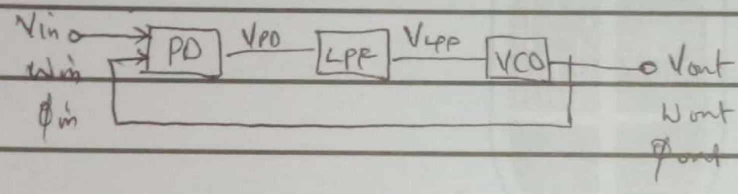




In the figure above, the two inputs to the phase detector as depicted as square waves.

$$\phi_0 = \frac{V_1}{K_D} - \frac{W_1 - W_0}{K_D K_0}$$

(4) PLL Dynamic response:



(5) Lock range: Range of input signal frequencies over which the loop remains locked once it has captured the input signal. This can be limited either by the phase detector or the VCO frequency range.

(a) If limited by phase detector:

$0 < \phi < \pi$ is the active range where lock can be maintained.

(b) The lock range could also be limited by the tuning range of the VCO. Oscillator tuning range is limited by capacitance ratios or current ratios and is finite. In many cases, the VCO can set the maximum lock range.

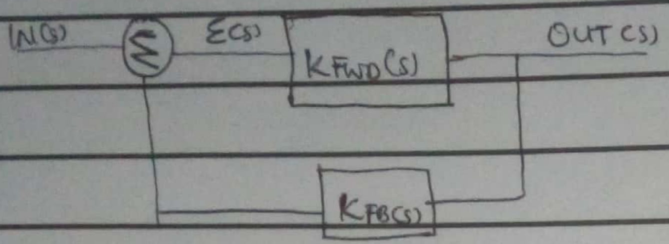
(6) Capture range; Range of input frequencies around the VCO center frequency onto which the loop will lock when starting from an unlocked condition.

(7) Approach: A frequency domain approach will be used, specifically describing transfer functions in the S-domain.

$$V_e(s) / \Delta\phi = K_D$$

$$\phi_{out}(s) / V_{cont}(s) = K_0/s$$

PLL is a feedback system



Loop Gain : $T(s) = K_{FWD}(s)\, K_{FB}(s)$

Transfer function : $\dfrac{OUT(s)}{IN(s)} = H(s) = \dfrac{K_{FWD}(s)}{1+T(s)}$

$$T(s) = \frac{k'(s+a)(s+b)\ldots}{s^n (s+\alpha)(s+\beta)\ldots}$$

ORDER = The order of the polynomial in the denominator

TYPE = n (the exponent of the s factor in the denominator)

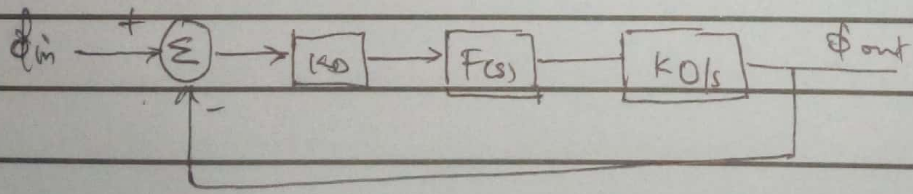
PHASE ERROR = $E(s) = \dfrac{IN(s)}{1+T(s)}$

(2)

STEADY STATE ERROR = $E_{ss} = \lim_{s\to 0}[s E(s)] = \lim_{t\to\infty} E(t)$

Frequency and Phase tracking loop:

(3)



Transfer function : $H(s)$ = Forward Path gain / [1 + T(s)]

with Feedback = 1

$H(s) = T(s) / [1 + T(s)]$

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{K_D K_O F(s)/s}{1 + K_D K_O F(s)/s}$$

Phase Error Function:

$$E_s = \phi_{in} - \phi_{out} = \frac{s\,\phi_{in}}{s + K_D K_O F(s)}$$