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COURSE: EEE 524 ANALOG DESIGN and APPLICATIONS

ASSIGNMENT

ANALOG MULTIPLIERS

Non Linear: Nonlinear operations on continuous-valued analog signals are often required in instrumentation, communication, and control system design; These operations include

* Rectification
* Modulation
* Demodulation
* Frequency translation
* Multiplication
* Division.

In analog-signal processing the need often arises for a circuit that takes two analog inputs and produces an output proportional to their product. Such circuits are termed analog multipliers.

The most commonly used techniques for performing multiplication and division within a monolithic integrated circuit are

* The emitter-coupled pair: This is shown in to produce output currents that were related to the differential input voltage by;

∆Ic=Ic1-Ic2=IEE tanh(Vid/2TT)

This relationship is plotted and shows that the emitter coupled pair by itself can be used as a primitive multiplier

Or assuming;

(Vid/2VT)<<1, =∆Ic=IEE(Vid/2VT)



* Gilbert multiplier cell: This is a modification of the emitter-coupled cell, which allows four-quadrant multiplication. The Gilbert multiplier cell is the basis for most integrated circuit balanced multiplier systems. The series connection of an emitter-coupled pair with two cross-coupled, emitter coupled pairs produces a particularly useful transfer characteristic.



There are three main application of Gilbert cell depending of the V1 an V2 range:

1. If V1<VT& V2<VT then; tanh(V1,2/2VT)=V1,2/2VT, and it works as multiplier
2. If one of the inputs of a signal that is large compared to VT, this effectively multiplies the applied small signal by a square wave, and acts as a modulator.
3. If both inputs are large compared to VT, and all six transistors in the circuit behave as non-saturating switches. This is useful for the detection of phase differences between two amplitude-limited signals, as is required in phase-locked loops, and is sometimes called the phase-detector mode.
* Two-quadrant restriction: Thus we have produced a circuit that functions as a multiplier under the assumption that Vid is small, and that Vi2 is greater than VBE(on). The latter restriction means that the multiplier functions in only two quadrants of the Vid - Vi2 plane, and this type of circuit is termed a two-quadrant multiplier. The restriction to two quadrants of operation is a severe one for many communications applications, and most practical multipliers allow four-quadrant operation.

PHASE LOCKED LOOP CIRCUITS (PLL)

1. A PLL is a feedback system that includes a VCO, phase detector, and low pass filter within its loop. Its purpose is to force the VCO to replicate and track the frequency and phase at the input when in lock. The PLL is a control system allowing one oscillator to track with another. It is possible to have a phase offset between input and output, but when locked, the frequencies must exactly track.

Φout(t) = Φin(t) + Const

Ꙍout (t) = Ꙍin(t)

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Of course, phase and frequency are interrelated by:

Ꙍ(t)= dφ/dt

Φ(t)= Φ(0) + Ѕt0Ꙍ(tI)dtI

Applications: There are many applications for the PLL, but we will study

* Clock generation
* Frequency synthesizer
* Clock recovery in a serial data link
1. Phase detector: These compares the phase at each input and generates an error signal, ve(t), proportional to the phase difference between the two inputs. KD is the gain of the phase detector (V/rad). As one familiar circuit example, an analog multiplier or mixer can be used as a phase detector. Recall that the mixer takes the product of two inputs.

V0 (t)=K0 [Φout(t)- Φin(t)]

1. Voltage controlled oscillator VCO: In PLL applications, the VCO is treated as a linear, time-invariant system. Excess phase of the VCO is the system output.

Φout =K0 Ѕt-∞ Vcont dtI

The VCO oscillates at an angular frequency, ωout. Its frequency is set to a nominal ω0 when the control voltage is zero. Frequency is assumed to be linearly proportional to the control voltage with a gain coefficient KO or KVCO (rad/s/v).

Ꙍout = Ꙍ0 + K0 Vcont



In the figure above, the two inputs to the phase detector are depicted as square waves.

1. PLL dynamic response: To see how the PLL works, suppose that we introduce a phase step at the input at t = t1.

Φin = Ꙍ1 t + Φ0 + Φ1 U (t-t1)

1. Lock Range: Range of input signal frequencies over which the loop remains locked once it has captured the input signal. This can be limited either by the phase detector or the VCO frequency range.
* If limited by phase detector: 0 < φ < π is the active range where lock can be maintained. For the phase detector type shown (Gilbert multiplier or mixer), the voltage vs. phase slope reverses outside this range. Thus the frequency would change in the opposite direction to that required to maintain the locked condition.

Ve-max = ± KD π/2

When the phase detector output voltage is applied through the loop filter to the VCO,

∆ωout – max = ± KV π/2 = ωL (lock range)

 where KV = KO KD, the product of the phase detector and VCO gains.

 This is the frequency range around the free running frequency that the loop can track. Doesn’t depend on the loop filter does depend on DC loop gain

* The lock range could also be limited by the tuning range of the VCO. Oscillator tuning range is limited by capacitance ratios or current ratios and is finite. In many cases, the VCO can set the maximum lock range.
1. Capture range: Range of input frequencies around the VCO center frequency onto which the loop will lock when starting from an unlocked condition. Sometimes a frequency detector is added to the phase detector to assist in initial acquisition of lock.

You will see later that the loop filter bandwidth has an effect on the capture range.

1. Approach: We will discuss the details of phase detectors and loop filters as we proceed. But, at this point, we will treat the PLL as a linear feedback system. We assume that it is already “locked” to the reference signal, and examine how the output varies with the loop transfer function and input. A frequency domain approach will be used, specifically describing transfer functions in the s-domain.

Ve(s)/∆φ = KD

 φout(s)/Vcont(s) = KO /s

 Note that the VCO performs an integration of the control voltage and thus provides a factor of 1/s in the loop transfer function. Because of this, a PLL is always at least a first order feedback system.



Loop Gain: T(s) = KFWD(s)KFB(s)

Transfer Function: OUT(s)/IN(s) = H(s) = KFWD(s)/1 + T(s)

The Loop gain can be described as a polynomial: T(s) = K1(s + a)(s+b)……/S󠄭 (s + ά)(s + β)

ORDER = The order of the polynomial in the denominator

TYPE = n (the exponent of the s factor in the denominator)

PHASE ERROR: There is no frequency error when the loop is locked

* Input frequency = output frequency

But, it is possible to have a phase error for some input transient phase conditions. The phase error must remain bounded in order to keep the loop locked. To analyze in the frequency domain, we assume a sinusoidal phase variation at the input

PHASE ERROR = ε(s) = IN(s)/1 + T(s)

TRANSIENT PHASE ERROR

* Inverse Laplace transform of ε(s)

Now, let’s look more closely at how the phase error is affected by the type of transient phase signal at the input of the Type I PLL.

Frequency ramp. We could do the same exercise for a frequency ramp (Doppler shift). This gives an unlimited steady state error. So, a type I loop is not suitable for tracking a moving source.

Frequency and phase tracking loop: First we will consider the PLL with feedback = 1; therefore, input and output frequencies are identical. The input and output phase should track one another, but there may be a fixed offset depending on the phase detector implementation.



Root Locus: Since there are no zeros, the root locus represents the roots of the denominator of the closed loop transfer function. Set 1 + T(s) = 0 and solve for s as a function of KV.

Bandwidth: The loop 3 dB bandwidth is important for noise considerations. It is determined by ωn and ζ, so bandwidth must be determined in conjunction with the overshoot and settling time specifications. We find again that the formula is different for the case with a forward path zero as opposed to the feedback zero case that we discussed in the feedback lectures.

Phase Frequency Detector: The phase-frequency detector shown below is a widely used architecture in frequency synthesizers. As opposed to the XOR phase detector that we first considered, this one produces two outputs: QA and QB, or as is customary, UP and DOWN respectively.

Charge Pump Loop Filter An alternative loop filter implementation called the charge pump is widely used for many applications. It is very convenient to implement in CMOS.

* The PFD output produces UP (QA) and DOWN (QB) pulses whose width is proportional to the phase error.
* Charge pump current sources I1 and I2 must produce exactly equal currents. They charge and discharge the capacitor, CP, in discrete steps.
* If there is a static phase error ∆φ at the PFD input, the capacitor, C, will be charged indefinitely – therefore, the DC gain is infinite: an ideal integrator. So, we expect to have zero static phase error. This is unlike the type I loop which gave ∆φ = ∆ω/KV steady state phase error.
* The CP PLL will detect small phase errors and correct them as long as the frequency of the phase error (jitter frequency) is within the loop 3 dB bandwidth. This phase comparison occurs on every cycle.

Closed Loop Frequency Response: The closed loop frequency response can be evaluated from H(jω).

Third-order CP PLL

There is still one residual problem that we have overlooked. The phase detector produces pulses of variable width that activate the switches to either charge or discharge the capacitor CP. Now that we have added the resistor, however, we find that the control voltage coming out of the charge pump will jump up or down before settling to its steady state value. This occurs because you cannot change the voltage across a capacitor instantaneously, so the initial voltage drop occurs across RP, which then charges CP exponentially. This jumpy control voltage frequency modulates the VCO at the reference frequency, creating reference spurs. This is not such a big problem if N = 1 because the jump will be at the same frequency as the VCO. But, at larger N values, it creates sidebands and jitter. So, we need to fix this by adding a second capacitor, C2, whose function is to filter out the jumpy response of the series RC network. The magnitude of the reference spur sidebands is reduced by a factor of ωREF/ωC2. Unfortunately, however, C2 adds a third pole of finite frequency that will reduce the stability of the PLL. A look at the Bode plot verifies this.

PLL Phase Noise:We have considered how the bandwidth of the loop affects things like settling time and capture range. But it also plays a role in the PLL noise behavior. For frequency synthesis, we are interested in low phase noise. There are at least 2 main sources:

* Reference noise – usually small since we frequently use a crystal oscillator
* VCO noise – often high. We hope that the PLL will suppress most of the noise, at least close to the carrier.

The effect caused by each of these noise sources can be seen from the closed loop transfer functions.

SUMMARY: This application note describes the basic control system techniques required for phase-locked loop design. Criteria for the selection of the optimum type of loop and methods for establishing the desired performance characteristics are presented. A design example is illustrated in a step-by-step approach along with the comparison of the experimental and analytical results.