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MAT NO: 15/ENG04/016

PHASE LOCKED LOOP

What is a PLL?

A PLL can be defined to be a feedback system which includes a VCO, phase detector, and low pass filter within its loop. The VCO in a PLL I used to track and replicate the frequency and phase at the input when in lock. PLL is said also to be a control system which permits only one oscillator to track with anther.



Fig: Typical PLL

The PLL output is obtained from either Vcont (filtered VCO control voltage which is almost DC) or obtained from the output of the VCO pending on the application. The VCO output can be used as a local oscillator or to generate a clock signal for digital system. The input to the system can either be phase or frequency. We obtain the following equations from the above figure;



But then we should recall that both frequency and phase are interrelated by:



* The phase detector in the feedback system above compares the phase at each input and then goes ahead to generate an error signal, ve(t) which is proportional to the phase difference between to inputs. The phase gain KD is given as:



* The VCO is treated as a linear time-invariant system. The excess phase of the VCO is the system output. It Is given as:



* PLL Dynamic response: assuming we introduce a phase step at the time input to b e t=t, then we obtain the equation below.



* Lock Range: the range of input signal frequencies over which the loop remains locked once it has captured the input signal. It can also be said to be limited by the phase detector or the VCO frequency range. Let’s look at two conditions which are:
1. If limited by the phase detector



0<φ<π is the active angle where the lock can be maintained. In order to maintain the locked condition, the frequency would change in the opposite direction as shown below using the equation.

Ve-max=+\_KD (π/2)

But, when the phase detector output is applied to the VCO via the loop filter we then have the equation below:



KV=KOKD (product of phase detector and VCO gains)

1. The lock range could be limited by the tuning range of the VCO. The oscillator tuning range is limited by capacitance ratios and it’s finite. In other cases the VCO can be set to the maximum lock range.
2. Capture Range the range of frequencies around the VCO centre frequency onto which loop will lock when starting from an unlocked condition. A frequency detector is sometimes added to the phase detector to assist in initial acquisition of the lock.



Loop Gain: T(S) = KFWD(S)\*KFB(S)

Transfer Function: = KFWD(S)/1 + T(S)

But, the loop gain ca n be described as a polynomial given as:

T(S) = K’(s + a) (s + b)……. /Sn (s +α) (s +β)…

Phase Error

ε(s) = IN(s) / 1 + T(s)

Steady State Error

εss = lim[sε(s)] = lim ε(t)

s → 0 s → ∞

Frequency and Phase tracking Loop

Consider a PLL with feedback = unity (1); hence, input and output frequencies are identical. Also the input and output phase should track one another, but pending on the phase detector which is put to use, there may be a fixed offset.



Transfer Function: H(s) = forward path gain/ [1 + T(s)]

With unity feedback

H(s) = T(s) / [1 + T(s)]

H(s) =

Phase Error function:

εs = in - out =

ANALOG MULTIPLIERS

Analog multipliers finds its operation in various modes such as;

1. Rectification,
2. Modulation,
3. Demodulation,
4. Frequency translation,
5. Multiplication and
6. Division.

In analog-signal processing there is the need for a circuit that takes two analog inputs and produces an output proportional to their product. Such a circuit is said to be an analog multiplier.

Emitter-coupled Pair

This is the most common and a simple multiplier that has been put to use.



The circuit is shown to produce output currents that are related to the differential input voltages as shown below.

Ic1 =

Ic2 =

The current IEE is the bias current for the emitter-coupled pair. IEE can be made proportional to a second input with the addition of more circuitory. And as such the current IEE then becomes;

IEE = Ko (Vi2 – VBE(on)).

The differential output current is then also calculated as;

Ic =

Some other application areas of analog multiplier circuits are;

1. Two Quadrant restriction
2. Gilbert muktiplier cell

Below represents a complete analog multiplier.

