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EEE524 Assignment

A Summary on Analog Multipliers And Phase Locked Loops (PLL)

Analog Multipliers

An analog multiplier is a device that takes in two analog inputs and produces an output proportional to their product. Based on circuit designs, they find application in many areas such as simple multipliers, modulation and phase locked loops.

An example is the emitter-coupled pair as a simple multiplier. The emitter-coupled pair is designed to produce output currents that are related to the differential input voltage V_{id} by $\Delta I_C = I_{C1} - I_{C2} = I_{EE}(V_{id}/2V_T)$

where I_{EE} is the bias current, $I_{EE} = k_0 (V_{i2} - V_{BE})$

$$\therefore \Delta I_C = \frac{k_0 V_{id} (V_{i2} - V_{BE})}{2V_T}$$

It operates only as a two-quadrant multiplier which is not good enough for many communication applications so most multipliers allow four-quadrant.

Another example is the Gilbert's multiplier cell which is a modification of the emitter-coupled cell that allows four-quadrant multiplication. Series connection of an emitter-coupled pair with two cross-coupled pairs produces a differential output current:

$$\Delta I = I_{EE} \tanh(V_1/2V_T) \tanh(V_2/2V_T)$$

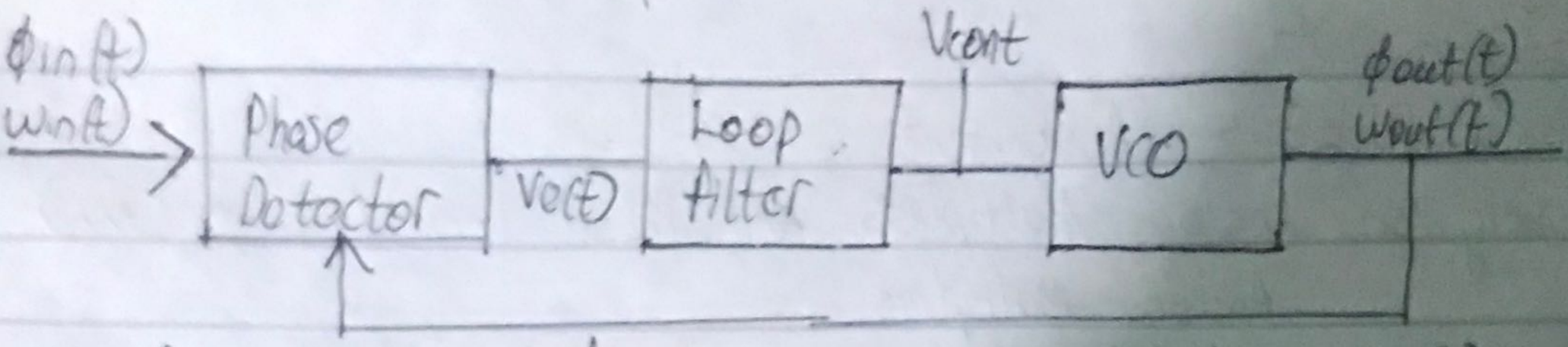
NB: It is therefore the product of the hyperbolic tangents of the two inputs

The applications of the Gilbertos cell which depend on V_1 and V_2 (inputs) range include:

i) If V_1 and V_2 are less than V_T, it works as a multiplier
ii) If one of the inputs is large compared to V_T, it multiplies the applied small signal by a square wave and acts as a modulator
iii) If both inputs are large compared to V_T, it is applied in the detection of phase difference between two input signals in phase locked loops.

Phase Locked Loops (PLL)

A Phase locked loop is a feedback system combining a voltage controlled oscillator (VCO), a phase detector and a low pass filter so as to make the VCO track the phase at the input when in lock.



Recall, phase and frequency are interrelated by $\omega(t) = \frac{d\phi}{dt}$

where $\omega(t) \rightarrow$ frequency and $d\phi \rightarrow$ Phase

$$\therefore \phi(t) = \phi(0) + \int_0^t \omega(t)\,dt$$

The main aim of phase locked loops (PLL) is to synchronise the output signal with the input signal in phase and frequency. Some of the areas where PLL are applied include clock generation, clock recovery and in frequency synthesizers. Some of the basic building blocks and criterias for PLL include!

1) Phase Detector: It compares the phase at each input and generates an error signal proportional to the phase difference between the two inputs

$$V_c(t) = K_D[\phi_{out}(t) - \phi_{in}(t)]$$

where $V_c(t)$ is the error signal

K_D is the gain of the phase detector

2) VCO: The VCO is set to a nominal frequency ω_0 when the control voltage is zero. It oscillates at an angular frequency ω_{out}

$$\omega_{out} = \omega_0 + K_0 V_{cont}$$

where K_0 is the VCO gain. (rad/s/V)

$$\phi_{out} = K_0 \int_{-\infty}^{t} V_{cont}\,dt$$

To maintain an arbitrary frequency output, a finite V_{cont} is required. As V_{ctr} changes, the frequency of osciliation also changes.

3) Loop filter: The loop filter smooths out the error signal from the phase detector. It removes the high frequency component (summation) from the output of the phase detector.

4) Capture Range: This is the range of input frequencies around the VCO nominal frequency onto which the loop can lock when starting from an unlocked condition.

5) Lock Range – This is the range of input frequencies over which the loop remains in lock condition once it has captured the input signal. Let's say for example the VCO is already locked to input frequency f and then the input frequency changes, the VCO will follow that frequency provided the input signal is within the lock range. But if the input signal goes out of the lock range, the VCO starts running at its nominal frequency and won't be able to lock to the input frequency until it is within the capture range.

6) Approach

If we assume the system is already locked to a reference (input) signal and examine how the output varies with the loop transfer function, we get

$$W_{out} = K_{VCO} \cdot V_{ctr}$$

where K_{VCO} is the oscillator gain

V_{ctr} is the control voltage.

NB! When the PLL is in lock, the V_{ctr} varies only around a small region around the lock point. Since we are interested in phase, and frequency is a time derivative of phase, we get

$$\phi_{VCO} = \frac{1}{s} \cdot F_{VCO} = \frac{1}{s} W_{out}$$

$$\therefore \phi_{VCO} / \phi_{out} = K_{VCO}/s \cdot V_{ctr}$$

$$\therefore K_{VCO}(s) = \frac{\phi_{out}(s)}{V_{ctr}(s)}$$

Recall $K_D = \frac{\Delta\phi}{V_e(t)}$

The loop gain is a combination of the foward and feedback gains which can be given by

$$T(s) = K_D(s) \cdot H(s) \cdot K_o(s)$$

NB.: There is no frequency error when the the loop is locked. ie input frequency = output frequency

But it is possible to have some phase error for some input transient conditions.

phase error $\varepsilon(s) = \frac{IN(s)}{1+T(s)}$

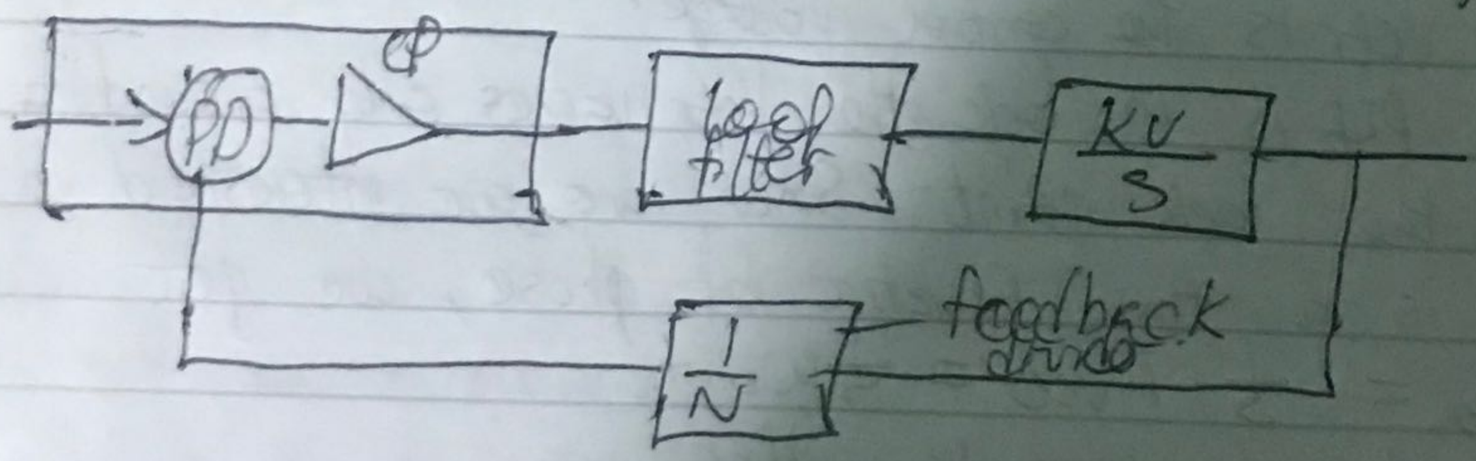
where $IN(s)$ is the input signal and $T(s)$ is the loop gain.
NB: There is only transient phase error for a phase step. The filter will return to the same value after the phase step is completed. The frequency will be the same before and after the step.

$$\phi_{in}(s) = \frac{\Delta\theta}{s}$$

The steady-state phase error is zero.
For a frequency step, $\phi_{in}(s) = \frac{\Delta\omega}{s^2}$

while steady state error $\varepsilon_{ss} = \frac{\Delta\omega}{K_V}$

for frequency ramp, the steady state error is unlimited, so a charge pump loop filter can be integrated into the loop. A common example of this application is in synthesizer PLL.



By making the divider N programmable, we can tune the VCO frequency with other integer N architecture or fractional-N architecture.