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Flip-Flop applications: Edge-triggered flip flop is versatile devices used in a wide variety of application including counting, storing of binary data, transferring binary data from one location to another. Application put to use is the sequential circuits. Sequential circuits is one in which is the outputs follow a predetermined sequence of states, with a new state occurring each time a clock pulse occurs.

Flip-Flop Synchronization: Some digital system have synchronous in their operation because most of the signal will change state in synchronism with clock transitions. They have external signal that is not synchronized to clock which called asynchronous. Asynchronous signal are caused as a result of a human operator’s actuating an input switch at some random time relative to clock signal. It’s randomness can produce unpredictable and undesirable results.

Detecting an Input sequence: In some situations, an output is to be activated only when the input are activated in a certain sequence.

Data storage and Transfer: It’s the most common use of flip flop for the storage of data or information. Data can be numerical values (e.g binary, numbers, BCD-coded decimal numbers) or a wide variety of types of data that have been encoded in binary. Data are generally stored in groups of FF’s called register. The operation most often performed on data that are stored in a register is the data transfer operation. It involves the transfer of data from one register to another.

Parallel Data Transfer

Serial data Transfer: Shift Registers –is a group of FF’s arranged so that the binary numbers stored in FF’s are shifted from one FF to the next for every clock pulse.

Hold Time Requirement : The shift register arrangement, it is necessary that the FFs have a very small hold time requirement because there are times when the J, K inputs are changing at about the same time as the CLK transition

Serial Transfer Between Registers: The three bit shift register connected so that so the content of X register will be serially transferred   
(shifted) into register Y. We are using Flip flop for each shift register because this requires few connections from J-K flip-flops.

Shift-Left Operation: The FFs can just as easily be connected so that information shift from right to left. There is no general advantage of shifting in one direction over another. The direction chose by a logic designer will often be dictated by nature of application.

Parallel Versus Serial Transfer: The parallel transfer is the transferred simultaneously upon the occurrence of a single transfer of a asingle command pulse, no matter how many bits are being transferred. Series transfer is the complete transfer of N bits of information requires N clocks pulses. Parallel transfer is faster than Serial transfer.

In parallel transfer, the output of each FF in register Y. In serial transfer, only the last FF in register X is connected to register Y. In general, then the parallel transfer requires more interconnection between the sending register (X) and the receiving register (Y) than does serial transfer. This difference becomes more critical when a greater number of bits of information are being transferred. This is an important consideration when the sending and receiving registers are remote from each other because it determines how many lines (wires) are needed for transmission of the information.

Frequency Division and Counting : FF has it’s J and K input at the 1 level, so that it will change states (toggle) whenever the signal on its CLK input goes from HIGH to LOW. The clock pulses are applied only to the CLK input of FF Q0. While output Q0 is connected to the CLK input of FF Q1, and output Q1 is connected to the CLK input of FF Q2. The following point should be noted:

1. Flip-flop Q0 toggles on the negative-going transition of each input clock pulse> Thus, the Q0 output waveform has a frequency that is exactly one half of the clock pulse frequency.
2. Flip-flop Q2 toggles each time the Q1 output goes from HIGH to LOW Thus, the Q2 waveform has one-half the frequency of Q1 and therefore one-eighth of the clock frequency.
3. Flip-flop Q2 toggles each time the Q1 output goes from HIGH to LOW. Thus, the Q2 waveform one-eighth of the clock frequency.
4. Each FF output is square wave (50% duty cycle).

MOD Number: MOD number has 8 different states. Which could be referred as to as a MOD-8 counter. MOD number indicates the number of states in counting sequence. If a fourth FF were added, the sequence of states would count in binary from 0000 to 1111, a total of 16 states.it would be called MOD-16 counter. The MOD number of a counter also indicates the frequency division obtained from the last FF. For instance, a four bit counter has four FFs, each representing one binary digit(bits) and so it’s a MOD-24 = MOD-16 counter. It can therefore count up to 15 ( = 24 – 1). It can also be used to divide the input pulse frequency by a factor of 16 ( the MOD number).

COUNTERS AND REGISTERS

Signal Flow: It is conventional in circuit schematics to draw the circuit (whenever possible) so that the signal flow is from left to right, with inputs on the left and outputs on the right. In this chapter, we will often break with this convention, especially in diagrams showing counters. The CLK inputs of each FF are on the right, the outputs are on the left, and the input clock signal is shown coming in from the right. We will use this arrangement because it makes the counter operation easier to understand and follow. FF is the rightmost most FF and FF D is the leftmost FF If we adhered to conventional left to right signal flow, we would have to put FF A on the left and FF D on the right, which is opposite to their position in the binary number that the counter represent. In some of the counter diagrams later in the chapter, we will employ the conventional left to right signal signal flow so that you will get used to seeing it.

MOD number: MOD number is generally equal to number of states that the counter goes through in each complete cycle before it recycles back to its starting states. The MOD number can be increased simply by adding more FFs to the counter. The counter must be able to count as many as one thousand items

Frequency Division: In basic counter each FF provides an output waveform that is exactly half the frequency of the waveform at its CLK input.

Propagation Delay In Ripple Counters: Ripples counters is the simplest type of binary counters because they requires a few component to produce a given counting operation. They do, however, have one major drawback, which is caused by their principle of operation.

Parallel Counters: The problem encountered with ripple counters are caused by the accumulated FF propagation delay. The FFs do not all change states simultaneously in parallel with the input pulses.

Circuit Operation: The counting sequence shows that the flip-flop must change states at each NGT. For this reason, its J and K inputs are permanently HIGH so that it will toggle on each NGT of the clock input.

Advantage of synchronous Counter over Asynchronous

In a parallel counter, all of the FFs will change states simultaneously. This is they are all synchronized of the NGTs of input clock pulses. Unlike the asynchronous counters, the propagation delay of the FFs do not add together to produce the overall delay.

Actual ICs

There are many synchronous IC counters in both the TTL and the CMOS logic families. Some of the most commonly used devices are:

* Synchronous decade counters
* Synchronous MOD-16 counters