Ejalonibu Oluwabusayo Mary

15/eng02/019

COE 506 ASSIGNMENT

**PROGRAMMABLE LOGIC DEVICES (PLD)**

PLD sometimes referred to as Field Programable logic devices (FPGA ) can be customed configured to create any desired digital circuit, from simple logic gate to complex digital systems.

There has been a lot of advancement in the development technology of PLD. The old devices could only handle a few inputs and outputs, now the new devices can handle hundreds of inputs and outputs.

PLD’s can be described as being one of the three different types :

* Simple Programmable Logic Devices (SPLDs)
* Complex Programmable Logic Devices (CPLDs)
* Field Programable logic devices (FPGA )

CPLDs and FPGAs are referred to as HIGH-Capacity programmable Logic Devices (HCPLDs). The programmable technologies of PLD are based on various types of semiconductor memory.

FUDAMENTALS OF PLD CIRCUITRY

Each of the four OR gates can produce an output that is a function of the two-input variable, A and B. Each output function is programmed with the fuses located between the AND gate and each of the OR gates. The figure below explains the above statement graphically.



Figure 1: FUNDAMENTALS OF PDF CIRCUITRY

With all the links initially intact, each OR output will be a constant 1, this is shown below;



Each of the four outputs O1, O2, O3, and O4 can be programmed to be any function of A and B by selectively blowing the appropriate fuses. PLD’s are designed so that a blown OR input acts as a logic 0, for example, looking at the diagram above, if fuses 1 and 4 are blown at OR gate 1, the O1 output becomes,



PLD SYMBOLOGY

PLD manufacturers have adopted a simplified symbolic representation of the internal circuitry of these devices. Below is a diagram of the simplified version of the FIGURE 1 , above.



Figure 2: SIMPLIFIED PLD SYMBOLOGY

In the above diagram the output is given as,



PLD ARCHITECTURE

PLD architecture includes, PROMs, Programmable Array Logic, Field Programmable Logic Array.

**PROM**: the architecture of programmable circuits in the previous section, involves programming the connections to the OR Gate. The AND Gates are used to decode all the possible combinations of the input variables.

For any input combination, the corresponding row is activated ( HIGH). If the OR input is connected to that row , a HIGH appears at the OR output, if the input is not connected, a LOW appears at the OR output.

**PAL**: this was created to fix the in adequacies of PROM in the implementation of SOP expressions.

The structure is similar to that of PROM, but in the PAL, inputs to the AND gates are programmable ,whereas the inputs to the OR gates are hard-wired.

**FPLA**: it uses a programmable AND array as well as a programmable OR array. It is more flexible than the PAL architecture but it is not accepted widely by engineers. It is mostly in state machine design where a large number of product terms are needed in each SOP expression.