**FLIP-FLOP**

Flip-Flop Applications

Edge-triggered flip-flop can be found in the following applications:

1. Counting
2. Storing of Binary Data
3. Transferring of Binary Data

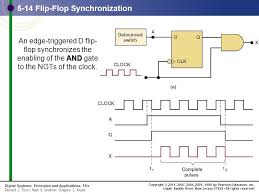
Flip-Flop Synchronization

Synchronous:

This means when the signals change their states with respect to the clock transitions. In the synchronous logic circuits, an electronic oscillator generates a repetitive series of equally spaced pulses called the clock signal. The clock signal is applied to all the memory elements in the circuit, called flip-flops. The output of the flip-flops only changes when triggered by the edge of the clock pulse, so changes to the logic signals throughout the circuit all begin at the same time, at regular intervals synchronized by the clock. The output of every other memory element in a circuit is usually described as the state of the circuit. The state of a synchronous circuit changes only with respect to the clock pulse.

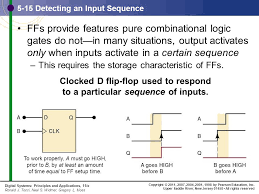
Asynchronous:

This means when an external signal that isn’t synchronized to the clock affects the change of states. There is no clock signal, and the state of the circuit changes as soon as the inputs change. Since asynchronous circuits don't have to wait for a clock pulse to begin processing inputs, they can be faster than synchronous circuits, and their speed is dependent only by the propagation delays of the logic gates.



HOW INPUT SEQUENCE CAN BE DETECTED

This can be achieved by using the storage characteristics of Flip-Flops. Like for example an AND gate can be used to determine when two inputs get HIGH with respect to one of the inputs getting high first. A clock can be used to achieve this.

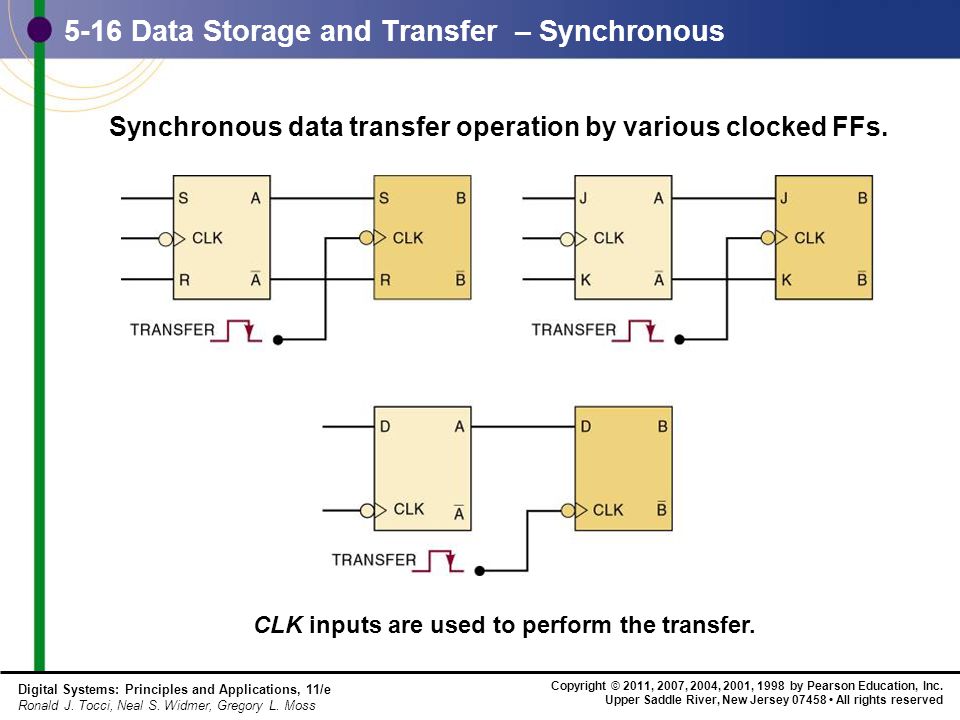


DATA STORAGE AND TRANSFER

This is one of the most common use of Flip-Flops

The operation must be performed on data that are stored in a FF or a register. Involves transfer of data from one register of FF to another.

Below are different ways:



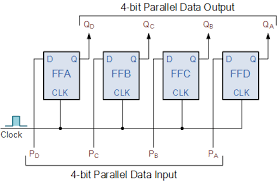
First diagram is data transfer done using SR Flip-Flops

Second diagram is data transfer done using JK Flip-Flops

Third Diagram is data transfer done using D Flip-Flops

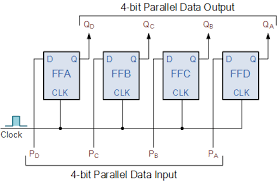
Parallel Data Transfer

This is called parallel because the contents of Pd, Pc, Pb and Pa are transferred simultaneously into Qd, Qc, Qb and Qa respectively.



SERIAL DATA TRANSFER: SHIFT REGISTERS

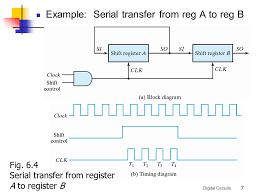
A shift register is a group of FFs arranged so that the binary numbers stored in the FFs are shifted from one FF to the next for every clock pulse.



HOLD TIME REGISTER

In this shift register arrangement, it is necessary that the FFs have a very small hold time requirement because there are times when the J, K inputs are changing at about the same times as the CLK transition.

SERIAL TRANSFER BETWEEN REGISTERS



FREQUENCY DIVISION AND COUNTING

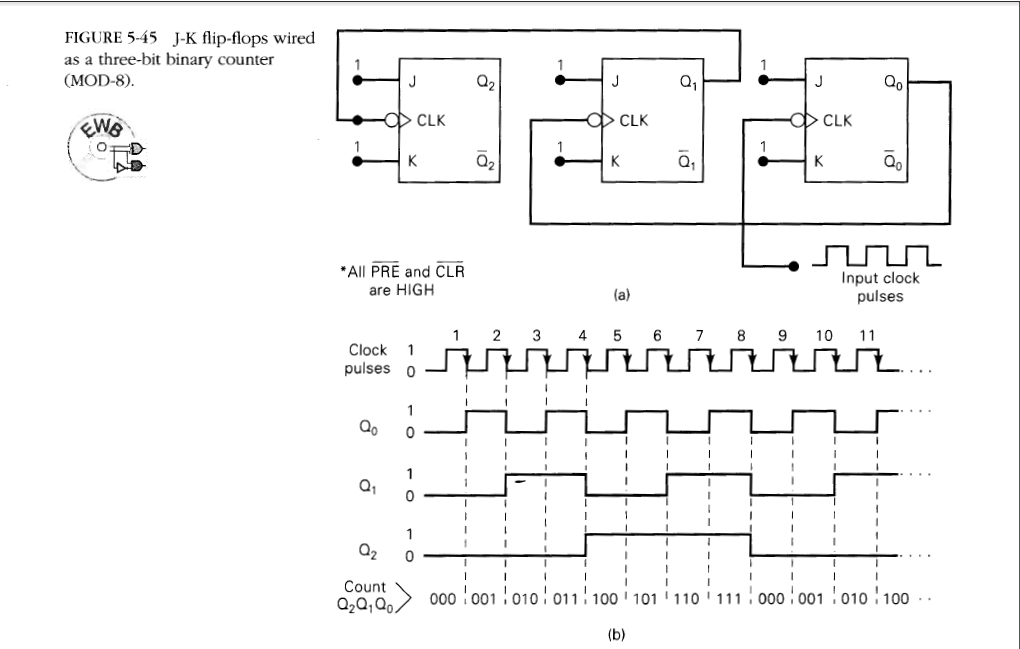
**FREQUENCY DIVISION:**

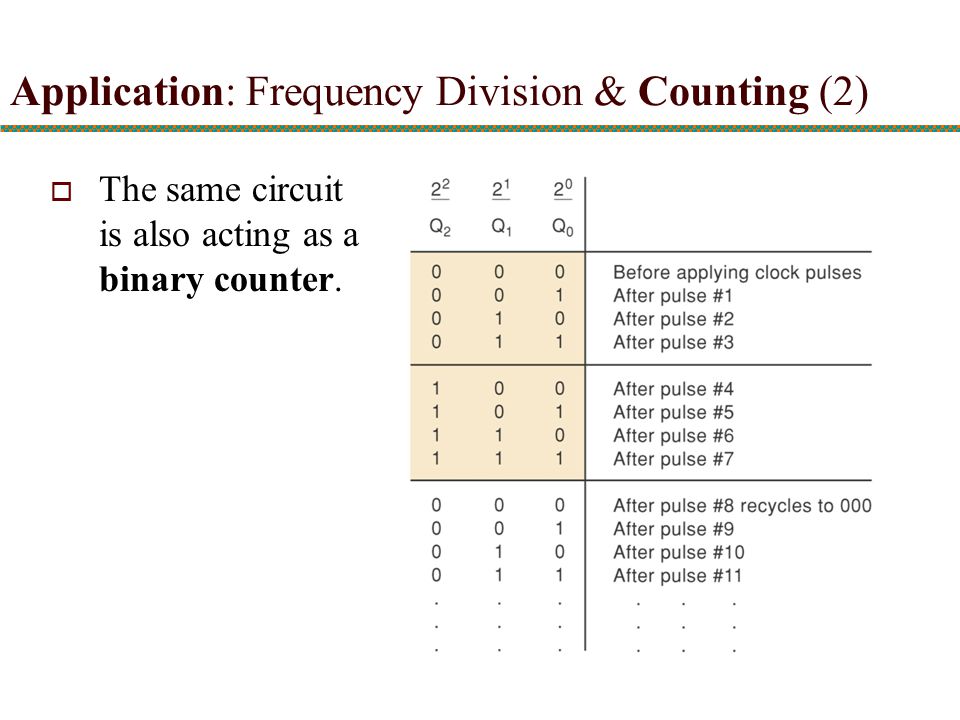
For frequency division, toggle mode flip-flops are used in a chain as a divide by two counter.

The final output clock signal will have a frequency value equal to the input clock frequency divided by the MOD number of the counter. Such circuits are known as “divide-by-n” counters. Counters can be formed by connecting individual flip-flops together and are classified according to the way they are clocked.

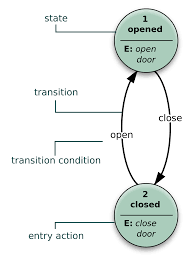
**FREQUENCY COUNTING**:

The basic idea of making a frequency counter is to count the number of cycles of the input in one second. We can keep one counter that keeps counting the rising/falling edges of the input signal. Then we can read the value of this counter once in a second and then clear it. The value we read from the counter is nothing but the frequency of the input signal.





STATE TRANSISTOR DIAGRAM



Each circle represents one possible state as indicated by the value inside the circle.

Each arrow indicates how one state changes from one state to another.

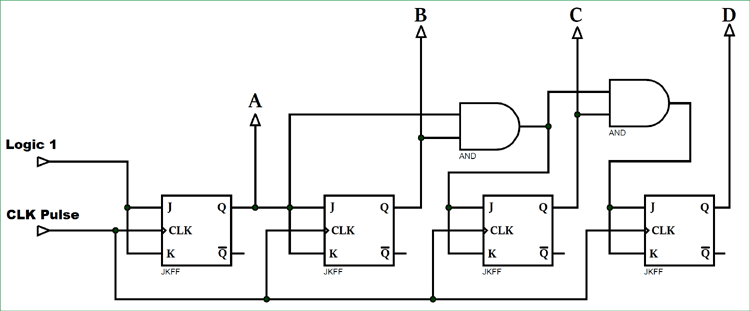
Synchronous Counter

**What is a Counter?**

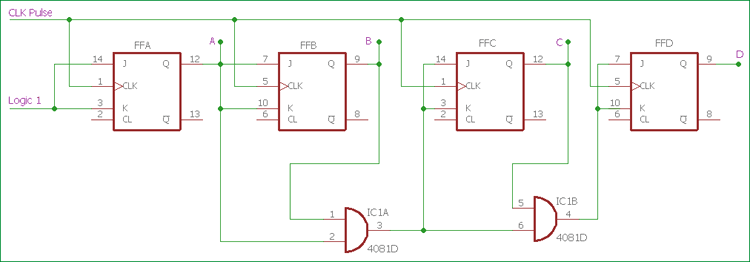
A counter is a device which can count any particular event on the basis of how many times the particular event(s) is occurred. In a digital logic system or computers, this counter can count and store the number of time any particular event or process have occurred, depending on a clock signal. Most common type of counter is sequential digital logic circuit with a single clock input and multiple outputs. The outputs represent binary or binary coded decimal numbers. Each clock pulse either increase the number or decrease the number.

**Synchronous Counter**

Synchronous generally refers to something which is coordinated with others based on time. Synchronous signals occur at same clock rate and all the clocks follow the same reference clock. In synchronous counter, the clock input across all the flip-flops use the same source and create the same clock signal at the same time. So, a counter which is using the same clock signal from the same source at the same time is called Synchronous counter.



**Synchronous Up Counter**

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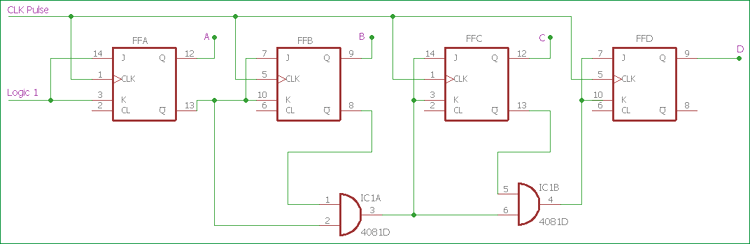
In the above image, the basic Synchronous counter design is shown which is Synchronous up counter. A 4-bit Synchronous up counter start to count from 0 (0000 in binary) and increment or count upwards to 15 (1111 in binary) and then start new counting cycle by getting reset. Its operating frequency is much higher than the same range Asynchronous counter. Also, there is no propagation delay in the synchronous counter just because all flip-flops or counter stage is in parallel clock source and the clock triggers all counters at the same time.

The external clock is directly provided to all J-K Flip-flops at the same time in a parallel way. If we see the circuit, the first flip-flop, FFA which is the least significant bit in this 4-bit synchronous counter, is connected to a Logic 1 external input via J and K pin. Due to this connection, HIGH logic across the Logic 1 signal, change the state of first flip-flop on every clock pulse.

Next stage, the second flip-flop FFB, input pin of J and K is connected across the output of the first Flip-flop. For the case of FFC and FFD, two separate AND gate provide the necessary logic across them. Those AND gates create logic using the input and output from the previous stage flip-flops.

We can create the same counting sequence used in the Asynchronous counter by making a situation where each flip-flops change its state depending on whether or not all preceding flip-flops output is HIGH in logic. But in this scenario, there will be no ripple effect just because all flip-flops are clocked at the same time.

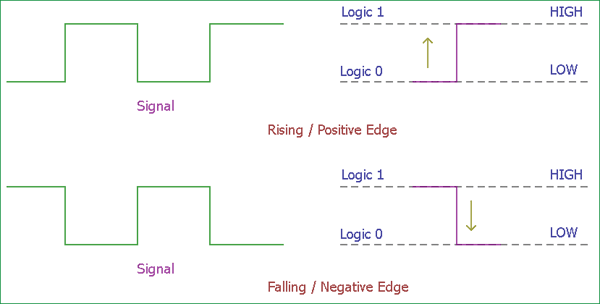
**Synchronous Down Counter**

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Slight changes in AND section, and using the inverted output from J-K flip-flop, we can create Synchronous Down Counter. A 4-bit Synchronous down counter start to count from 15 (1111 in binary) and decrement or count downwards to 0 or 0000 and after that it will start a new counting cycle by getting reset. In synchronous down counter, the AND Gate input is changed. First Flip-flop FFA input is same as we used in previous Synchronous up counter. Instead of directly feeding the output of the first flip-flop to the next subsequent flip-flop, we are using inverted output pin which is used to give J and K input across next flip-flop FFB and also used as input pin across the AND gate. Same as like the previous circuit, two AND gates are providing necessary logic to the next two Flip-flops FFC and FFD.

**Trigger Pulse related information**

There are two type of edge triggered flip-flops available, Positive edge or Negative edge.



Positive Edge or Rising Edge flip-flops count one single step when the clock input changes its state from Logic 0 to Logic 1, in other term Logic Low to Logic High.

On the other hand, Negative Edge or falling Edge flip-flops count one single step when the clock input changes its state from Logic 1 to Logic 0, in other term Logic High to Logic Low.

The advantages of the Synchronous counter are as follows-

1. It’s easier to design than the Asynchronous counter.
2. It acts simultaneously.
3. No propagation delay associated with it.
4. Count sequence is controlled using logic gates, error chances are lower.
5. Faster operation than the Asynchronous counter.

Although there are many advantages, one major disadvantage of working with Synchronous counter is that it requires a lot of extra logic to perform.

**Use of Synchronous Counter**

Few applications where Synchronous counters are used-

1. Machine Motion control
2. Motor RPM counter
3. Rotary Shaft Encoders
4. Digital clock or pulse generators.
5. Digital Watch and Alarm systems.

Asynchronous counters

Asynchronous counters are those whose output is free from the clock signal. Because the flip flops in asynchronous counters are supplied with different clock signals, there may be delay in producing output.

The required number of logic gates to design asynchronous counters is very less. So they are simple in design. Another name for Asynchronous counters is “Ripple counters”.

**Different types of Asynchronous counters**

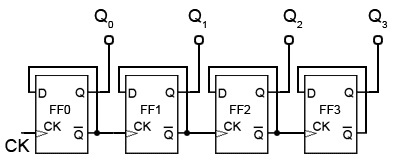
There are many types of Asynchronous counters available in digital electronics. They are:

1. 4 bit synchronous UP counter
2. 4-bit synchronous DOWN counter
3. 4-bit synchronous UP / DOWN counter

**Asynchronous 4-bit UP counter**

A 4 bit asynchronous UP counter with D flip flop is shown in above diagram. It is capable of counting numbers from 0 to 15. The clock inputs of all flip flops are cascaded and the D input (DATA input) of each flip flop is connected to a state output of the flip flop.

That means the flip flops will toggle at each active edge or positive edge of the clock signal. The clock input is connected to first flip flop. The other flip flops in counter receive the clock signal input from Q’ output of previous flip flop. The output of the first flip flop will change, when the positive edge on clock signal occurs.



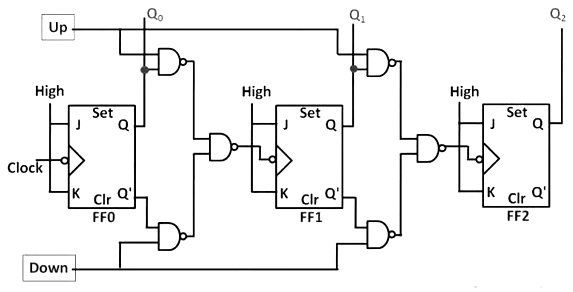
**Asynchronous 4-bit DOWN counter**

A 4-bit asynchronous DOWN counter is shown in above diagram. It is simple modification of the UP counter. 4 bit DOWN counter will count numbers from 15 to 0, downwards. The clock inputs of all flip flops are cascaded and the D input (DATA input) of each flip flop is connected to logic 1.

That means the flip flops will toggle at each active edge (positive edge) of the clock signal. The clock input is connected to first flip flop. The other flip flops in counter receive the clock signal input from Q output of previous flip flop, rather than Q’ output.

**Asynchronous 3-bit up/down counters**

By adding up the ideas of UP counter and DOWN counters, we can design asynchronous up /down counter. The 3 bit asynchronous up/ down counter is shown below.



**UP Counting**

If the UP input and down inputs are 1 and 0 respectively, then the NAND gates between first flip flop to third flip flop will pass the non-inverted output of FF 0 to the clock input of FF 1. Similarly, Q output of FF 1 will pass to the clock input of FF 2. Thus the UP /down counter performs up counting.

**DOWN Counting**

If the DOWN input and up inputs are 1 and 0 respectively, then the NAND gates between first flip flop to third flip flop will pass the inverted output of FF 0 to the clock input of FF 1. Similarly, Q output of FF 1 will pass to the clock input of FF 2. Thus the UP /down counter performs down counting.

The up/ down counter is slower than up counter or a down counter, because the addition propagation delay will have added to the NAND gate network.

**Advantages**

1. Asynchronous counters can be easily designed by T flip flop or D flip flop.
2. These are also called as Ripple counters, and are used in low speed circuits.
3. They are used as Divide by- n counters, which divide the input by n, where n is an integer.
4. Asynchronous counters are also used as Truncated counters. These can be used to design any mod number counters, i.e. even Mod (ex: mod 4) or odd Mod (ex: mod3).

**Disadvantages**

1. Sometimes extra flip flop may be required for “Re synchronization”.
2. To count the sequence of truncated counters (mod is not equal to 2n), we need additional feedback logic.
3. While counting large number of bits, the propagation delay of asynchronous counters is very large.
4. For high clock frequencies, counting errors may occur, due to propagation delay.

**Applications of Asynchronous Counters**

1. Asynchronous counters are used as frequency dividers, as divide by N counters.
2. These are used for low power applications and low noise emission.
3. These are used in designing asynchronous decade counter.
4. Also used in Ring counter and Johnson counter.
5. Asynchronous counters are used in Mod N ripple counters. EX: Mod 3, Mod 4, Mod 8, Mod 14, Mod 10 etc.