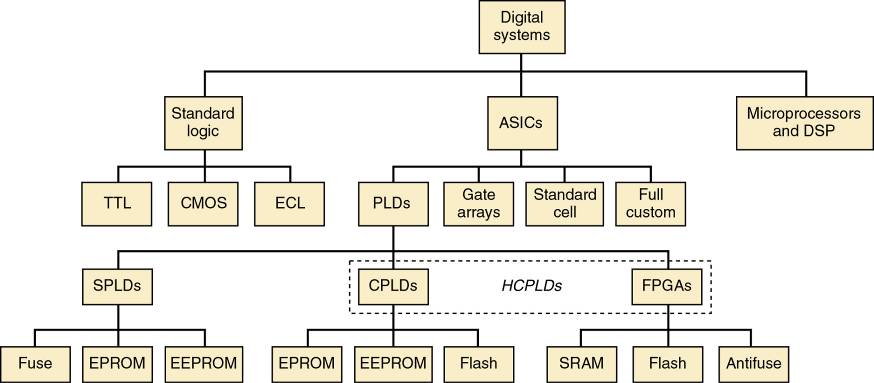
**Samuel Ibitogbe**

**15/eng02/029**

**VHDL**

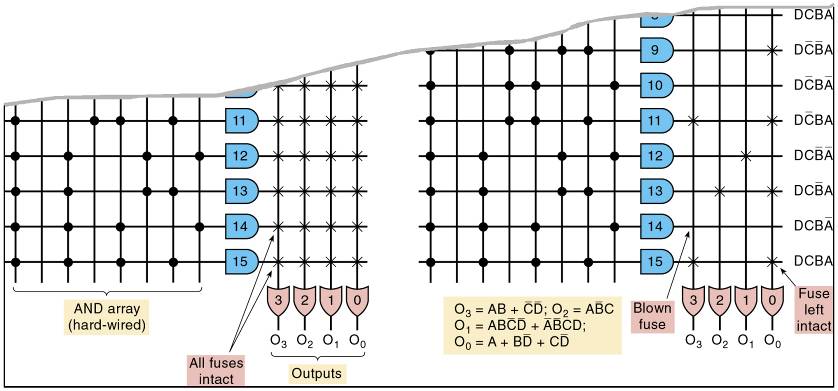
**PROGRAMMABLE LOGIC DEVICE ARCHITECTURE**

* **Digital System Family Tree**
* A digital system family tree showing most of the hardware choices currently available can be useful in sorting out the many categories of digital devices
* 

**Fundamentals of PLD Circuitry**

* **A device that be programmed by blowing the appropriate fuses at the input to the OR ar**
* **Manufacturers have adopted the simplified diagram symbols shown**
* **Gate arrays are ULSI circuits.**
  + **Logic functions are created by interconnections of hundreds of thousands of prefabricated gates.**
    - **A custom-designed mask is used—much like  
      the stored data in a mask-programmed ROM.**
  + **Individually less expensive than PLDs of comparable gate count.**
    - **Custom programming process is very expensive  
      and requires a great deal of lead time.**
* **Standard-cell ASICs use predefined logic function building blocks called cells to create  
  the desired digital system.** 
  + **A library of available cells is stored in a database.** 
    - **Design costs for standard-cell ASICs are higher  
      than for MPGAs—with greater lead time.**
* **Cell-based functions are designed to be much smaller than equivalent functions in gate arrays.**
  + **Allows for generally higher-speed operation and cheaper manufacturing costs.**
* **Full-custom ASICs are the ultimate ASIC choice.** 
  + **All components and the interconnections between them are custom-designed by the IC designer.**
  + **Requires a significant amount of time and expense, but it can result in ICs that can operate at the highest possible speed and require the smallest die area.** 
    - **Which significantly lowers manufacturing cost.**

**PLD Architectures**

* PROMs.
  + Fuses are blown to implement a SOP expression.
    - Bit map generation is made easier with general purpose logic compilers.
    - 
* Programmable array logic (PAL).
  + Every **AND** gate can be programmed to generate any desired product of four input variables.
* The PAL family also contains devices with variations of the basic SOP circuitry.
  + Channel SOP logic circuit to a D FF input and use one of the pins as a clock input, to clock all of the output flip-flops synchronously.
  + Field programmable logic array (FPLA)
  + Programmable **AND** as well as **OR** arrays.
  + Used in state machine applications where a large number of product terms are needed in each SOP expression.
  + Not as widely accepted by engineers
  + Generic array logic architecture (GAL).
  + Uses an EEPROM array in the programmable matrix that determines the connections.
  + The EEPROM switches can be erased and  
    reprogrammed at least 100 times.
  + GAL chips use a programmable output logic macrocell (OLMC).
  + Can be used as a generic, pin-compatible replacement for most PAL devices
  + **The Altera**
* I/O control blocks configure each I/O pin for input, output, or bi-directional operation.
* All I/O pins have a tristate output buffer that is:
  + Permanently enabled or disabled.
  + Controlled by one of two global output enable pins.
  + Controlled by other inputs or functions generated  
    by other macrocells.
* During in-system programming I/O pins will be tristated and internally pulled up to avoid board conflicts.

**The Altera Cyclone Series**

* Different architecture—based on the look up  
  table (LUT).
  + The LUT functions like a truth table for the logic function.
* SRAM devices that use LUT are generally classified as field programmable gate arrays (FPGAs).
* The LUT:
  + Is a portion of the programmable logic block that produces a combinational function.
    - The function can be output or registered.
  + Consists of FFs that store the truth table.
  + Is usually small, typically with 4 input variables.
  + Is basically, a 16 X 1 SRAM memory block.
* Has SRAM that must be loaded at PLD power up