Alamin Mohammed Nabil

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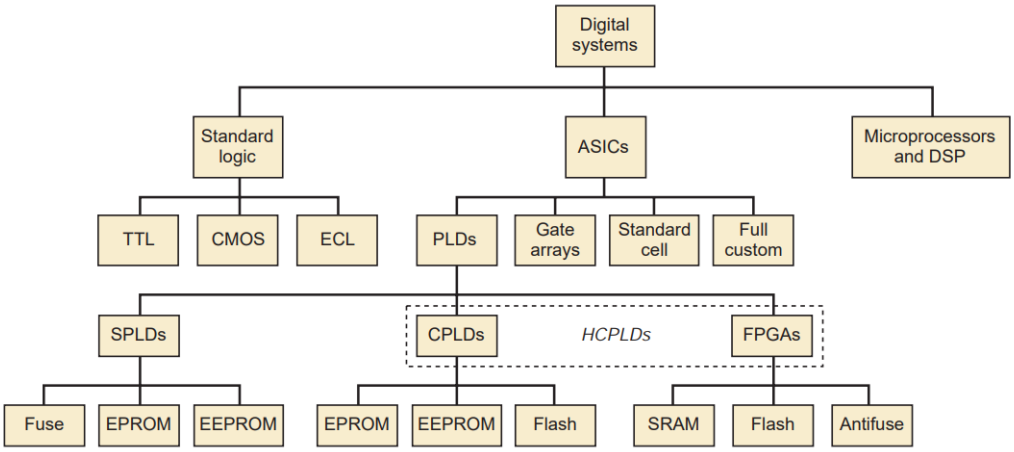
Programmable Logic Devices and Architectures

The First Category of standard logic devices are the basic functional components; gates, flipflops, decoders, etc. Available as MSI and SSI. With the Second Category, microcomputers/DSP systems, devices can be controlled electronically and data manipulated by executing a program of instructions. Hardware Solutions for digital design is always faster than a software solution. The Third category are application Specific integrated circuits (ASIC) i.e. ICs designed for specific purposes.

The categories of digital systems can be seen in tree below:



Programmable Logic Devices (PLDs) also called field programmable logic devices (FPLDs) can be custom configured to create a desired circuit for either complex or simple systems. PLDs are dynamic is nature as their architecture depends on its application, they can be Simple PLDs (SPLD), Complex PLDs (CPLD), Field Programmable Gate Array (FPGA). FPGAs and CPLDs are often called high capacity programmable logic devices (HCPLDs). Gate Arrays are ULSI

Circuits as logic functions can be created by interconnections of hundreds of thousands of fabricated gates, they are also less expensive compared to PLDs.

Standard ASICs use predefined logic function building blocks called cells to create the desired digital system, a cell-based function is smaller than the gate arrays of equivalent function thereby increasing operational speed and production costs. Full custom ASIC are custom designed by an IC designer and although they tend to be expensive they operate at high rates.

A Programmable Logic Device (PLD) circuitry is based on blowing out fuses of an array of OR gates. Manufacturers have simplified the design to make understanding easier:

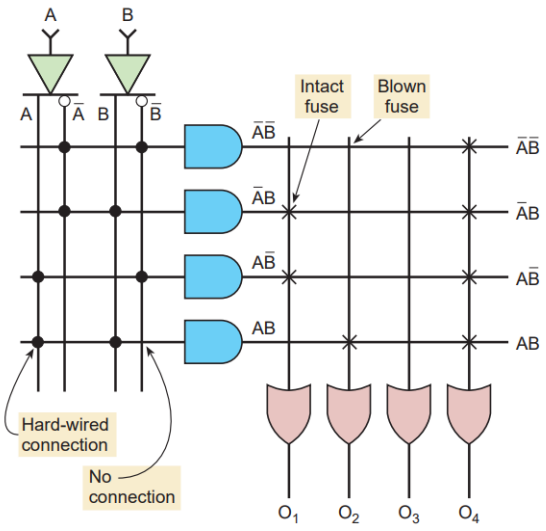


FIGURE 13-4 Simplified PLD symbology.

An architecture of the PLD is PROM in which the blown fuses tare used to perform an SOP (Sum of Product) operation. It also made bit map generation easier with general purpose logic compilers. Another Architecture is the Programmable Array Logic (PAL) where every AND gate can be programmed to generate a desired product of four inputs.

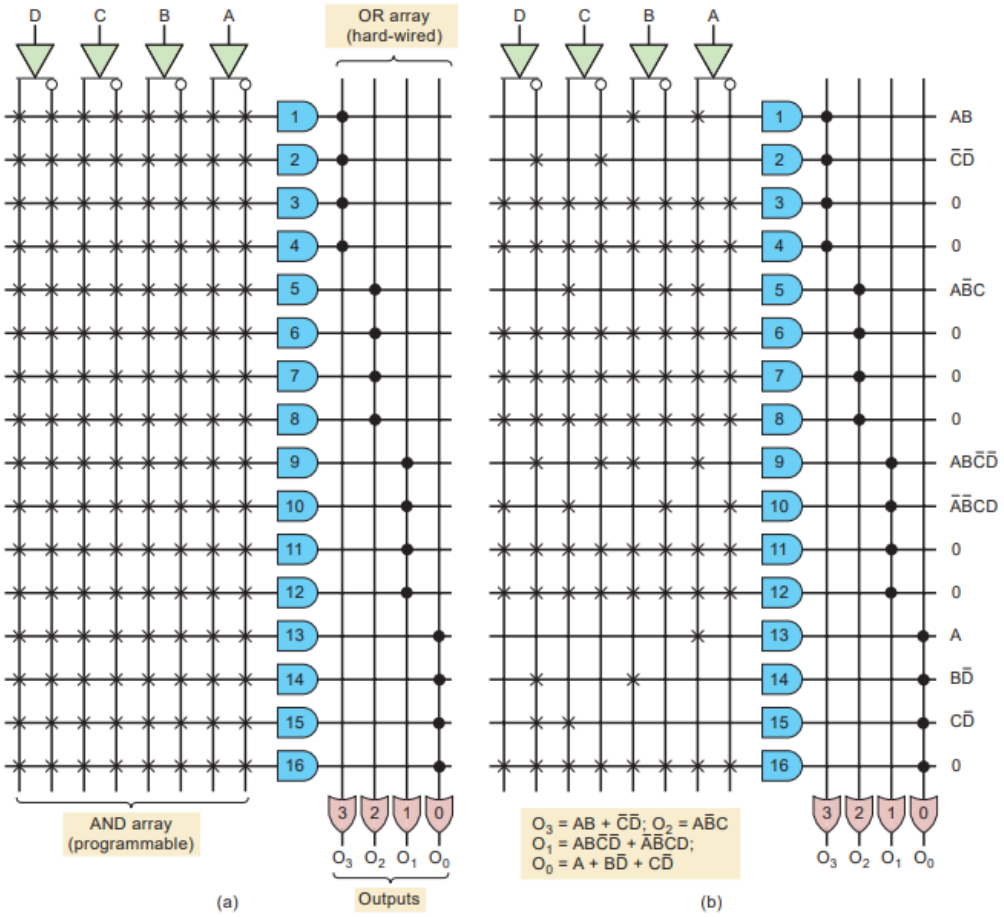


FIGURE 13-6 (a) Typical PAL architecture; (b) the same PAL programmed for the given functions.

These PALs also have variations that use the SOP one example is the registered PLD which uses D flipflop to clock all output flipflop synchronously. There is also the Field Programmable Logic Array (FPLA) PLD architecture though not accepted by engineers uses both programmable AND, OR gates which can be used for state machines. Then there is the Generic Array logic architecture (GAL) are very flexible as they can be used as a pin compatible replacement for most PAL device this is possible because an EEPROM array in a programmable matrix determines the connections possible, they use a programmable output logic macrocell (OLMC). The EEPROM switches can be erased and reprogrammed at least 100 times.

The Alterra EPM7128S CPLD is EEPROM based device in Altera MAX7000S CPLD family. Its structure is composed of Logic Array Blocks (LABS) and Programmable Interconnect Array (PIA). The LAB contains a set of 16 macrocells and looks very similar to a single SPLD device. Each macrocell consists of a programmable AND/OR circuit and a programmable register (flip-flop).