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15/ENG02/033
DIGITAL SYSTEM DESIGN WITH VHDL
C0E 506 ASSIGNMENT 2
May 11, 2020.

DIGITAL SYSTEM FAMILY TREE

A desired circuit functionality can be achieved using different types of digital hardware. The major digital system categories include standard logic, application-specific integrated circuits (ASICs) and microprocessor/digital signal processing (DSP) devices which have many subcategories.

Standard logic devices refers to the basic functional digital components (gates, decoders, etc.) that are SSI and MSI chips. The three major families of standard logic devices are TTL, CMOS and ECL, with CMOS being the most popular due to its low power consumption.

Microprocessor/digital signal processing (DSP) usually contain the various types of functional blocks and they can be controlled electronically and the data can be manipulated by executing a program of instructions that has been written, the major downfall of this is the speed.

Application-specific integrated circuits (ASICs) represents the hardware design solution for digital systems. The four subcategories are programmable logic devices, gate arrays, standard-cell and full-custom.

- **Gate array**s are ULSI circuits that offer hundreds of thousands of gates. The desired logic functions are created by interconnections of these prefabricated gates. They are also called mask-programmed gate arrays because a custom-designed mask for the specific application determines the gate interconnections just like the data stored in a mask programmed ROM.
- **standard-cell ASICs** use predefined logic functions building blocks called cells to create the desired digital systems. The IC layout of each cells has been designed previously, and a library of available cells is stored in a database.
- **full-custom ASICs** are considered the ultimate ASIC choice. All components (transistors, resistors, and capacitors) and the interconnections between them are custom-designed by the IC designer.

PLDs

These are devices that could be custom configured to create any desired logic gates to complex digital systems. This ASIC design is different from the other three, in the sense that PLDs are relatively cheaper to program in comparison to gate arrays, standard-cell and full-custom. PLDs have three different types namely:

- simple programmable logic devices (SPLDs)
- complex programmable logic devices (CPLDs)
- field programmable gate arrays (FPGAs)

CPLDs and FPGAs are often referred to high-capacity programmable logic devices (HCPLDs). The programming technologies for PLD devices are based upon their semiconductor memories. The amount of logic resources available is what differentiates the SPLDs from the HCPLDs

PLD SYMBOLOGY

The diagram below has 3 input variables, the input buffers are represented as a single buffer with two outputs, one inverted and one non-inverted. The connections from the input variable lines to the AND gate input are indicated as dots. The single row lines represents the multiple inputs to the AND gate. An X represents an intact fuse connecting a product line to one input of the OR gate. The absence of an X or a dot at any intersection represents a blown fuse. For an OR gate, blown fuses are pressumed to be LOW, and for AND gate inputs, they are seen as HIGH.

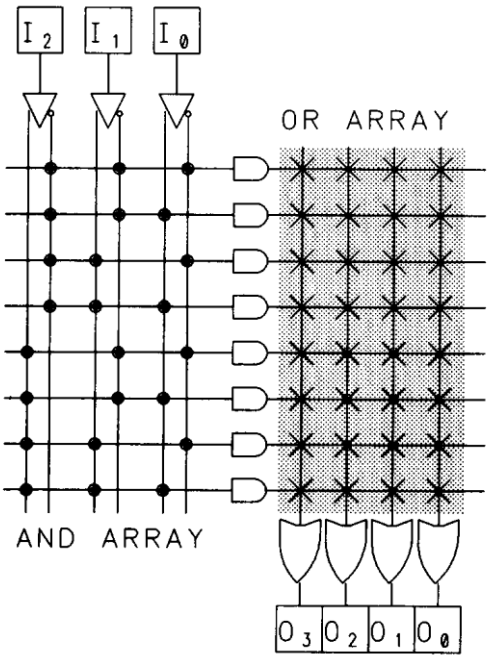

FIGURE 1: A PLD SYMBOLOGY.

PLDs ARCHITECTURE

The whole theory of PLDs has led to different architectural designs such as PROMs, programmable array logic (PAL) and field programmable array logic (FPAL).

PROMs

The architecture of programmable circuits involves programming the connection to the OR gate while the AND gates are used to decode all the possible combinations of the input variables. The PROM can generate any possible logic function of the input variables because it generates every possible AND product term. Any application that needs every input combination to be available is a good candidate for a PROM. A PROM is a programmable logic device.

Programmable array logic (PAL)

This has an AND and OR structure similar to a PROM but in the PAL, inputs to the OR gates are hardwired. This limits each output function to four product terms. If a function needs more than four, it can't be implemented. If less than 4 product terms are needed, the unneeded are made to be 0. The PAL family also contains devices with variations of the basic SOP circuitry, most PALs have a tristate buffer driving the output pin.

Field programmable array logic (FPAL)

This uses a programmable AND array as well as a programmable OR array. It is used mostly in state-machine design where a large number of product terms are needed in each SOP expression.

THE GAL 16V8 (GENERIC ARRAY LOGIC)

The GAL chip uses an EEPROM array to control the programmable connections to the AND matrix, allowing them to be erased and reprogrammed may times. This device has 8 dedicated

input pins, two special function inputs and 8 pins that can be used as input or outputs. The major components of the GAL devices are the input term matrix, the AND gates and the output logic macrocell (OLMCs). It has three different modes: simple mode, complex mode and registered mode. The GAL 16V8 is an affordable and versatile PLD chip.

THE ALTERA EPM7128S CPLD

This is an EEPROM-based device in the Altera MAX7000S CPLD family. The major structures in this family are logic array blocks (LABs) and programmable interconnect array (PIA). Logical signals are sent between LABs via PIA. The LAB contains a set of 16 macrocells which can share logic resources like unused AND gates and the PIA is a global bus that connects any signal source to any destination in the device. Only signals needed to produce the required functions for any LAB are fed into that LAB.