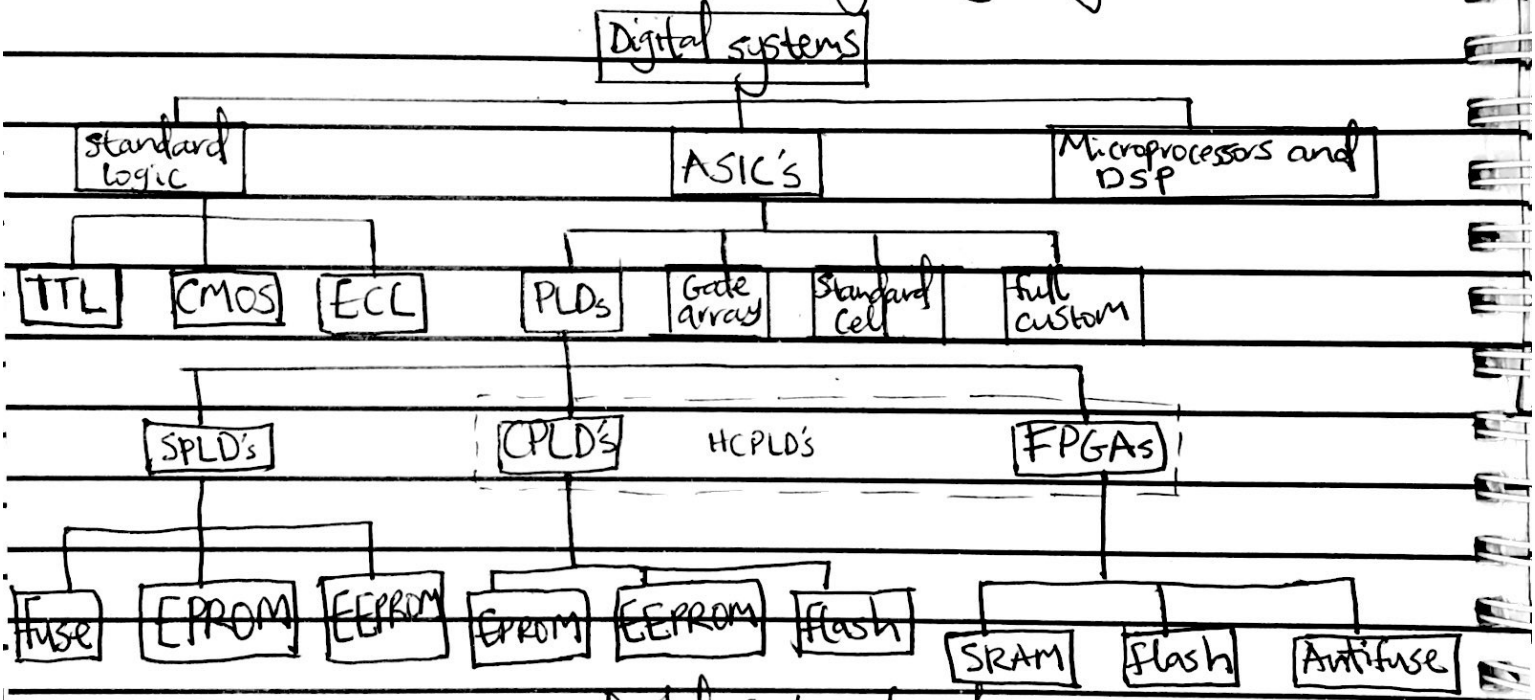
Agoyi Isaac Otuoze
15/ENG02/002
COE 502 Assignment

To design a product, the ~~digital~~ design engineering decisions must take factors such as necessary speed of operation for the circuit, cost of manufacturing, system power consumption, system size, amount of time available to design the product etc. Atimes, digital designs are combinations of hardware categories. The figure below, shows the hardware choices available in categorizing digital devices.



Digital System family tree

The standard logic devices are the basic components such as gates, flipflops etc. and are available as chips. Standard logic devices have three major families which are TTL, CMOS and ECL. Few designs apply TTL logic but many digital systems

contain TTL devices. CMOS is the most popular category because it consumes a lower amount of power. ECL technology is used for higher speed devices.

The Microprocessor/digital signal processing category have systems that can be controlled electronically and data can be manipulated by executing a program of instructions

The Application specific integrated circuits is designed for purpose of implementing a specific application. The programmable logic devices (PLD's) category can be customed to create any desired digital circuit from simple logic gates. Gate arrays are circuits that offer thousands of gates and a custom designed mask determines the gate interconnection. Standard cell ASICs use predefined building blocks (cells) to create the desired digital system. In full custom ASIC category, all components are custom designed by the IC designer.

PLD's, generally exists in three forms; simple programmable logic devices, complex programmable logic devices and field programmable gate arrays. SPLD's contain fewer gates than HC PLD's.

CPLD's are devices that combine an array of PAL type devices on the same chip. FPGA's consists of many relatively small and independent programmable logic modules that can be connected to create larger functions.

FUNDAMENTALS of PLD CIRCUITRY

The figure below is a PLD device where the four OR gates produce an output which is a function of two input variables A and B. The output is programmed with fuses between AND and OR gate. The AND outputs are called product lines and each of the product lines are connected to one of the four inputs of each OR gate.

$O_1 = \bar{A}\bar{B} + \bar{A}B + A\bar{B} + AB \Rightarrow \bar{A}(\bar{B}+B) + A(\bar{B}+B)$

$= \bar{A} + A \Rightarrow 1$

The four outputs can be reprogrammed by blowing the appopriate fuses to give: $O_1 = 0 + \bar{A}B + A\bar{B} + 0 + 0 = \bar{A}B + A\bar{B}$.

The OR outputs can be programmed in a similar manner to give a function desired.

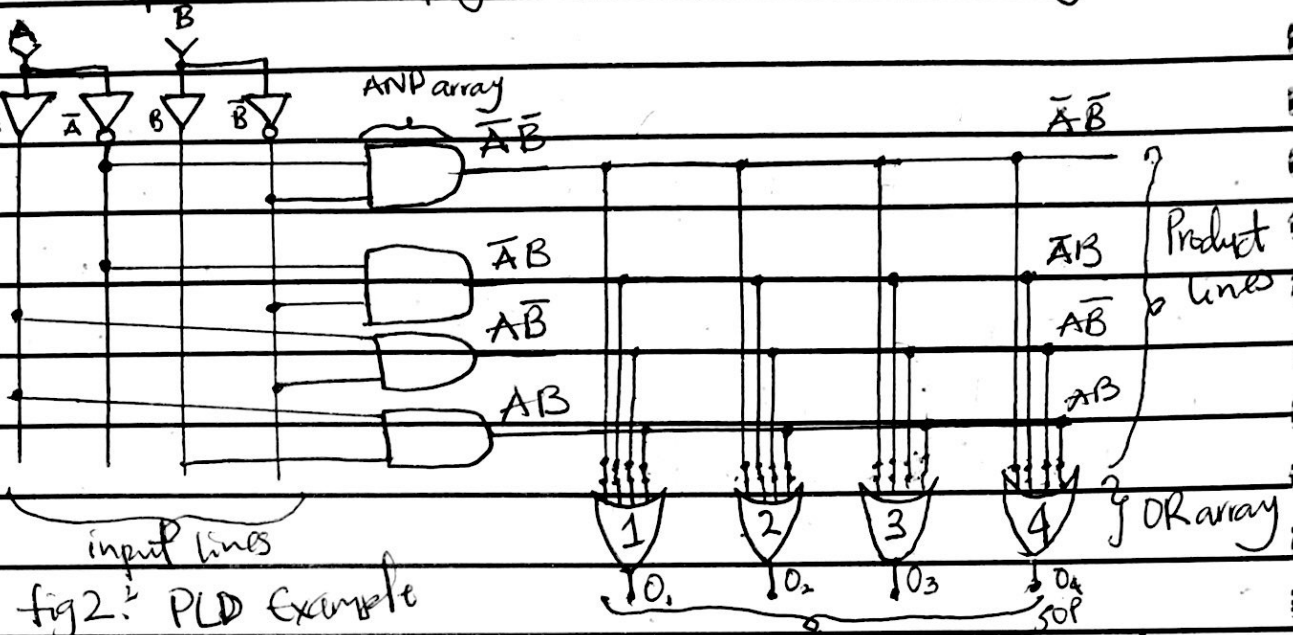


fig 2: PLD Example

X represents an intact fuse connecting a product line to OR gate. For OR gate inputs, the blown fuses are assumed to be LOW, and for AND gate inputs, blown fuses are HIGH. The outputs are programmed as: $O_1 = \bar{A}B + A\bar{B}$; $O_2 = AB$; $O_3 = 0$; $O_4 = 1$

A dot represents a blown fuse.

PLD ARCHITECTURES

The steps which PROM would be programmed to generate four specified logic functions starts by; constructing the truth table showing the desired O_3 output levels for all possible input combinations. Next, we write down the AND product for cases where output should be 1. The O_3 output is the OR sum of these products and all other output should be blown. Any application that requires every input combination to be available is good for PROM. PROM becomes impractical when a large

number of input variables must be accomodated.

PROGRAMMABLE ARRAY LOGIC:- The PAL has an AND and OR structure similar to a PROM but in the PAL, inputs to the AND gate are programmable whereas inputs to the OR gates are hardwired.

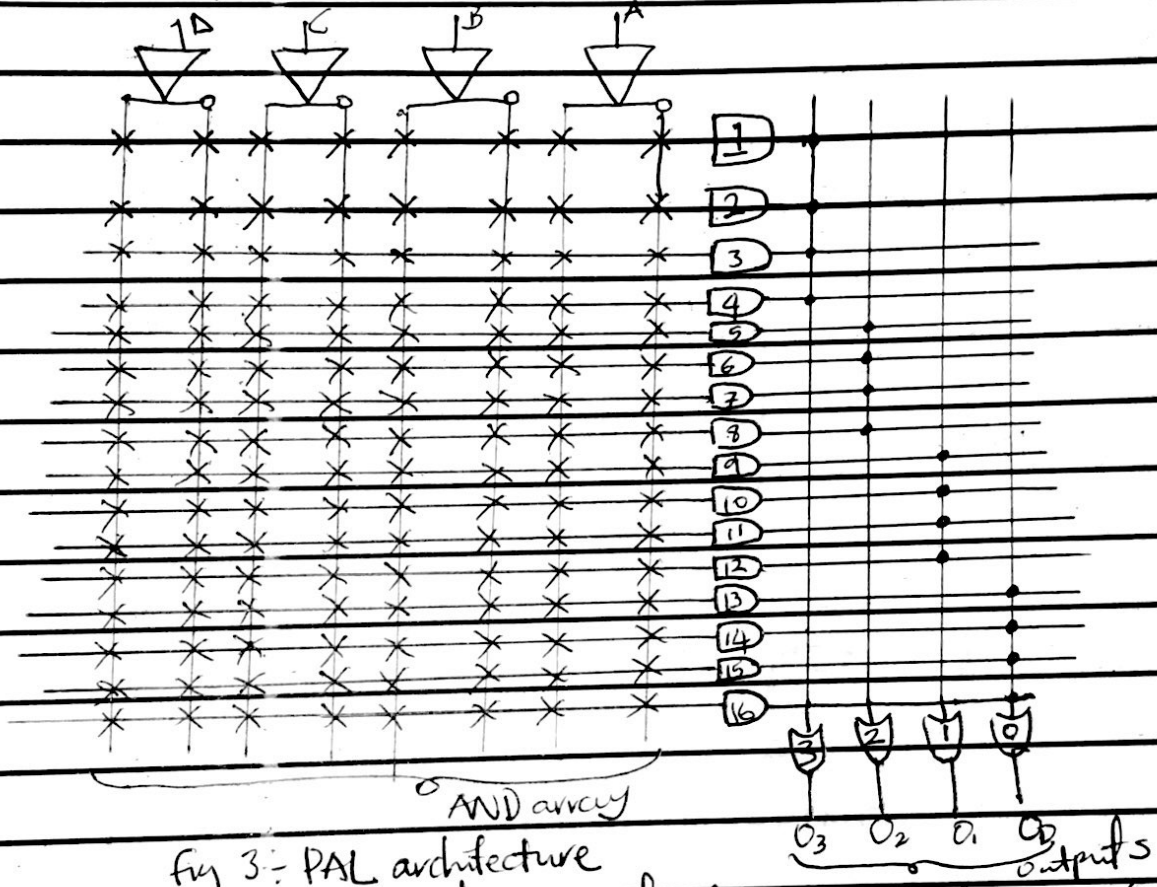


fig 3:- PAL architecture

The PAL is programmed to generate four logic functions, by first expressing the output as OR sum of four terms ($O_3 = AB + \bar{C}D + 0 + 0$). Next we program inputs to AND gates 1, 2, 3 and 4 so that they provide the correct product-terms to OR gate 3. An example of PAL family is PAL1618.

Field programmable logic Arrays are used in state machine design.

GENERIC ARRAY LOGIC:- is very similar to PAL devices but uses an EEPROM array to control programmable connections allowing them to be erased and reprogrammed at least 100 times. It contains special flip-flops