A SUMARIZED PAPER

ON

PROGRAMMABLE LOGIC DEVICE ARCHITECTURES

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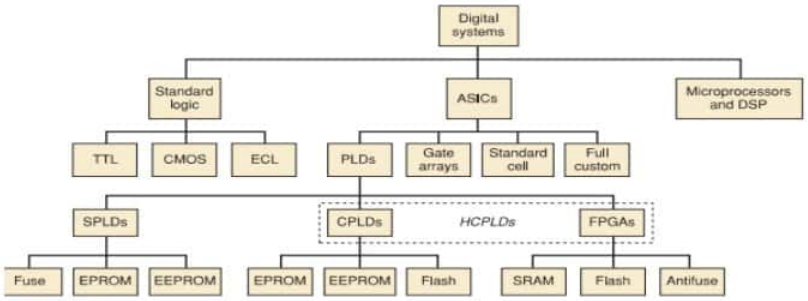
In the world today, there are a wide variety of digital systems (ranging from simple to complex), all which have their various applications. But currently in the technology market, the most conventional(ordinary) digital systems are not being applied with standard logic device chips containing only simple gates or MSI (Medium scale Integration) functions, Instead, Programmable Logic Devices (PLDs) are being used to create logic functions; meaning the same functionality can be obtained using just one integrated circuit rather than several logic chips. So, using PLD's means less power is required, less boards space and even lower cost when manufacturing. With the basic understanding on PLD's, an introduction will be made on the architectures of various families of PLD's.

DIGITAL SYSTEM FAMILY TREE



'IGURE 13-1 Digital system family tree.

The major digital system categories include; the Standard Logic Device, Application Specific Integrated Circuit (ASIC) and Digital Signal Processing (DSP) devices.

- The first category of **Standard Logic** Devices refers to the basic digital components (i.e. gates, flipflops, etc.) which are presented as SSI and MSI chips. These devices have been used for many years to design complex digital systems. Under the standard logic, there are major families: TTL, CMOS and ECL. Very few designs apply TTL logic, CMOS is the most popular standard logic family due to its low power consumption and ECL is applied for higher speed designs.
  Disadvantage of Category: Will require a lot of SSI and MSI chips
- The second category is **Microprocessor/ digital signal processing**. With DSP and microprocessors, devices can be controlled electronically.
  Disadvantage of Category: lacks speed.
- The third category is ASICs (Application Specific Integrated Circuits). Under this category there are four subcategories which include; PLD's, gate arrays, standard cell and full custom.
  The **programmable logic device** also referred to as **field programmable logic device** can be custom configured to create any digital circuit ranging from simple to complex.

The **Gate Arrays** which offers hundreds of thousands of gates are individually less expensive than PLD's, but its custom programming process is very expensive and requires a lot of lead time.

The **Standard cell ASIC's** uses predefined logic building blocks called "cells" to create the desired system. Design cost is higher and a greater lead time is needed for creation.

The **full custom ASIC's** are considered as the ultimate ASIC choice. Here all components and the interconnections between them are custom designed by the IC designer. This requires a lot of time and cost, but it results in highest speed of the IC's.

More on PLD's

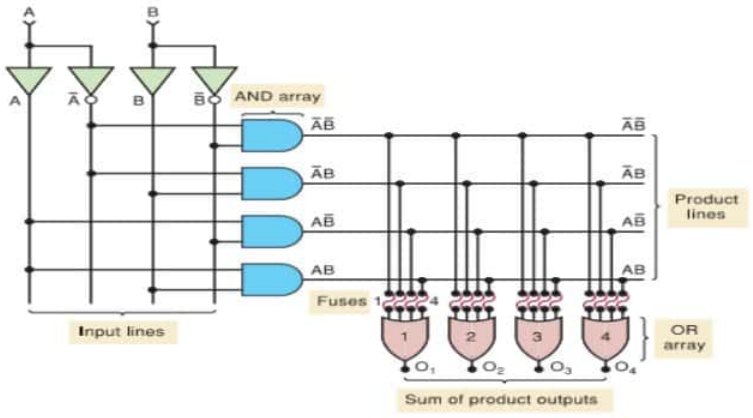
The development of PLD technology has advanced and is continuously doing so. From containing few hundred gates, devices can now contain few million gates. The old devices could only handle a few inputs and outputs and now there are PLD's that can handle hundreds of inputs and outputs.

Generally, PLD's can either be described as; **Simple Programmable Logic Devices (SPLD)**, **Complex Programmable Logic Devices (CPLD)** or **Field Programmable Gate Array (FPGA)**. Together, CPLD and FPGA are often referred to as **High Capacity Programmable Logic Devices** (HCPLD). Today, many small digital applications need only the resource of an SPLD (having 600 gates or less) due to its inexpensiveness and less complexity, but on the other hand, HCPLDs (having 1000- 100,000gates) provides circuit resources for complex digital systems. PLD didn't gain a wide acceptance with designers until the late-70s. With the development of ultraviolet erasable PROM came the EPROM based PLDs in the mid-80s.

FPGAs typically consists of many small independent programmable logic modules that are interconnected to create larger functions. The modules utilize a lookup table (LUT) to create a desired function.

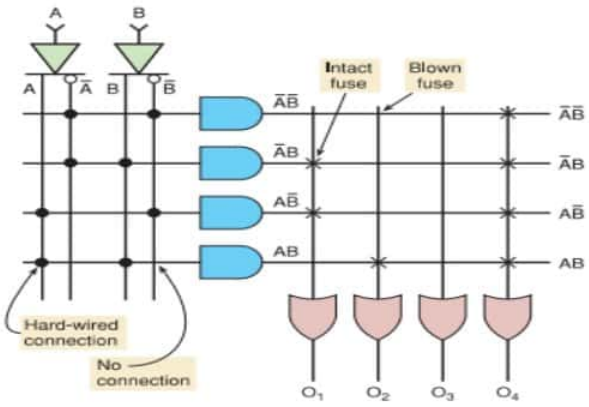
PLD CIRCUITRY (FUNDAMENTAL VS SIMPLIFIED SYMBOLS)

FIGURE 13-3 Example of a programmable logic device.



A)

FIGURE 13-4 Simplified PLD symbology.



B)

The diagrams above are examples of PLD circuitry. The first image (A) displays how circuits were made at the time (but later PLD manufacturers adopted a better way to represent PLD symbols as shown in fig (B).

The input buffers are now represented as a single buffer with two outputs and rather than have multiple lines going into the **AND & OR** Gates, it was modified to just a single line representing all 4 inputs. The connections from the input variables to the **AND** gates are presented as dots (the dots mean it is hand-wired). For the **OR** gate, an X represents an "intact fuse" between the product line (from the AND gate) to the inputs of the OR gate and the absence of an X or dot represents a "blown fuse" as seen in the figures above.

PLD ARCHITECTURES: PROM

Here the AND gates are used to decode all combinations of the input variables. For any given input combination, the corresponding row goes HIGH. If the OR input is connected to the row, the OR output is HIGH. If the input is not connected, the OR output will be LOW.

PROM can generate any possible logic function of input variable because it generates every AND product term.

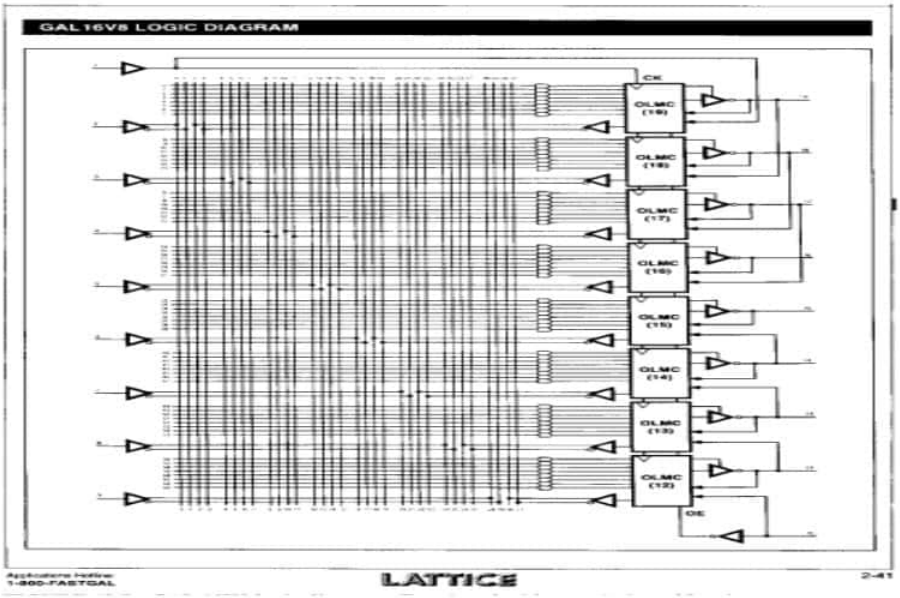
PROGRAMMABLE ARRAY LOGIC

The architecture of PAL differs slightly from PROM. The PAL has an AND and OR structure similar to the PROM, but in PAL the inputs to the AND gates are programmable and OR gates are hand-wired. This means that every AND gate can be programmed to generate any desired product of the four input variables and their complements, and each OR gate is hard wired to only four AND outputs. Note that many AND gates have their inputs fuses intact because they need to generate 0s (0s are only generated when there are unneeded AND products, when the AND products are fewer than four).

FIELD PROGRAMMABLE LOGIC ARRAY

This was the first nonmemory programmable logic device developed in mid-70s. it used both programmable AND & OR arrays and although it was more flexible than PLA architecture it was never accepted by the engineers. They are mostly used in state machine design where a large number of product terms are need in an SOP expression.

THE GAL 16V8 (GENERIC ARRAY LOGIC)



This device has a very similar architecture to PAL. It can even be used as a generic, pin compatible replacement for most PAL devices. The major components of the GAL devices are its input terms matrix; the AND gate and the output logic macrocells. The flexibility of GAL lies in its programmable logic output marocell. Though it has a lot of pins, the GAL16V8 is an inexpensive and versatile PLD chip.

THE ALTERA EPM7128S CPLD

This is an EEPROM based device in the ALTERA MAX7000s CPLD family. The major structures in this device are the logic array blocks (LABs) and the programmable interconnect array (PIA). A LAB consists of a set of 16 macrocells, and the EPM7128S has 128 macrocells arranged in eight LABs. A PIA is a bus that connects any signal source to any destination within the device, and all inputs to the MAX7000s device and all macrocells feed the PIA. The logic signals are routed between LABS through the PIA and up to 36 signals(significant) can feed the LABS via the PIA.