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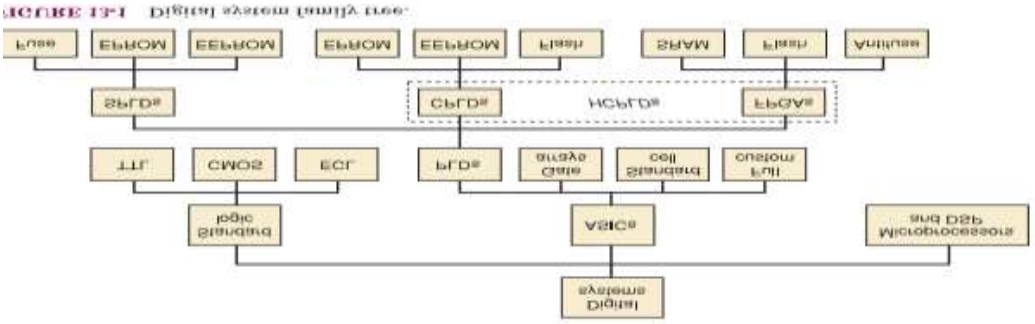
COE506 VHDL ASSIGNMENT (SUMMARY)

A **programmable logic device** (**PLD**) is an electronic component used to build reconfigurable digital circuits. Unlike integrated circuits (IC) which consist of logic gates and have a fixed function, a PLD has an undefined function at the time of manufacture.[1] Before the PLD can be used in a circuit it must be programmed (reconfigured) by using a specialized program.

In the world today, there are a wide variety of digital systems (ranging from simple to complex), all which have their various applications. But currently in the technology market, the most conventional(ordinary) digital systems are not being applied with standard logic device chips containing only simple gates or MSI (Medium scale Integration) functions, Instead, Programmable Logic Devices (PLDs) are being used to create logic functions; meaning the same functionality can be obtained using just one integrated circuit rather than several logic chips.

DIGITAL SYSTEM FAMILY TREE

Digital electronic circuits are usually made from large assemblies of logic gates, often packaged in integrated circuits. Complex devices may have simple electronic representations of Boolean logic functions.



The major digital system categories include; the Standard Logic Device, Application Specific Integrated Circuit (ASIC) and Digital Signal Processing (DSP) devices. The first category of **Standard Logic** Devices refers to the basic digital components (i.e. gates, flipflops, etc.) which

are presented as SSI and MSI chips. These devices have been used for many years to design complex digital systems. Under the standard logic, there are major families: TTL, CMOS and ECL. Very few designs apply TTL logic, CMOS is the most popular standard logic family due to its low power consumption and ECL is applied for higher speed designs.

A device programmer is used to transfer the boolean logic pattern into the programmable device. In the early days of programmable logic, every PLD manufacturer also produced a specialized device programmer for its family of logic devices

FUNDAMENTALS ON PLD CIRCUITRY

SRAM, or static RAM, is a volatile type of memory, meaning that its contents are lost each time the power is switched off. SRAM-based PLDs therefore have to be programmed every time the circuit is switched on. This is usually done automatically by another part of the circuit.

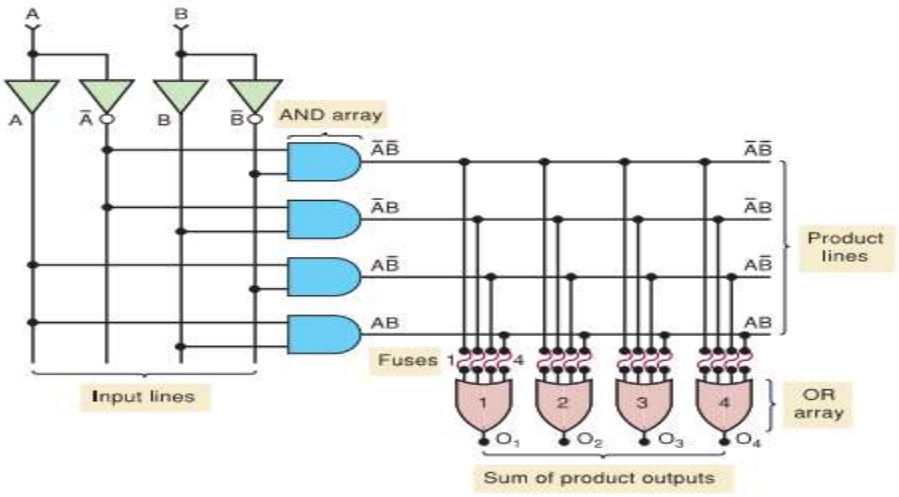


FIGURE 13-3 Example of a programmable logic device.

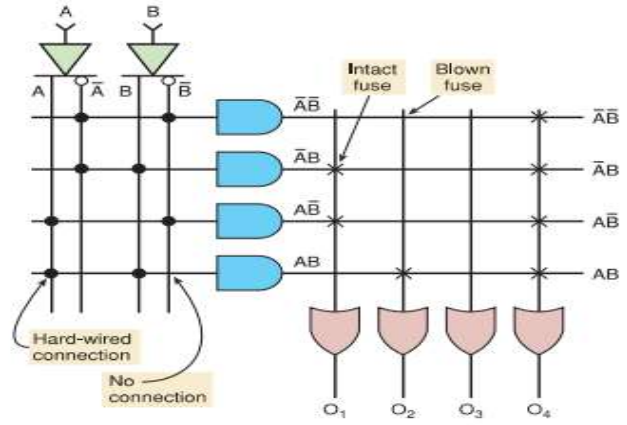


FIGURE 13-4 Simplified PLD symbology.

The diagrams above are examples of PLD circuitry. The first image (A) displays how circuits were made at the time (but later PLD manufacturers adopted a better way to represent PLD symbols as shown in fig (B).

PLD ARCHITECTURES (PROM)

The programmable logic plane is a programmable read-only memory (PROM) array that allows the signals present on the device pins, or the logical complements of those signals, to be routed to output logic macro cells.. PAL devices have arrays of transistor cells arranged in a "fixed-OR, programmable-AND" plane used to implement "sum-of-products" binary logic equations for each of the outputs in terms of the inputs and either synchronous or asynchronous feedback from the outputs.

PROGRAMMABLE ARRAY LOGIC

Programmable Array Logic (**PAL**) is a family of programmable logic device semiconductors used to implement logic functions in digital circuits introduced by Monolithic Memories, Inc. (MMI) in March 1978.[1] MMI obtained a registered trademark on the term PAL for use in "Programmable Semiconductor Logic Circuits". The trademark is currently held by Lattice Semiconductor.[2]

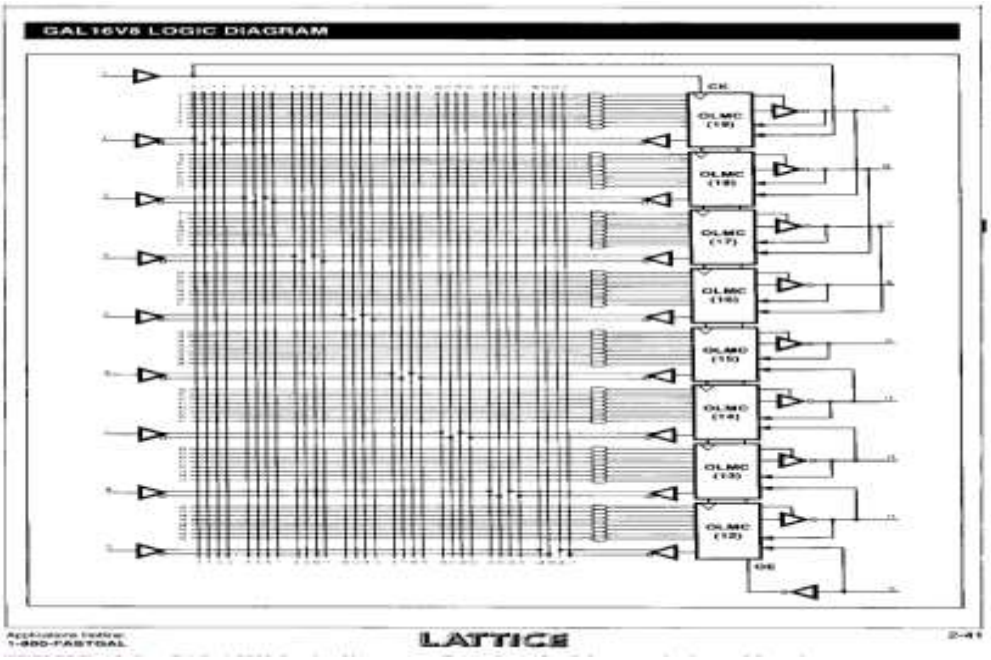
PAL devices consisted of a small PROM (programmable read-only memory) core and additional output logic used to implement particular desired logic functions with few components.

FIELD PROGRAMMABLE LOGIC ARRAY

A programmed logic array in which the internal connections of the logic gates can be programme d once in the field by passing high current through fusible links, by using avalanche-induced migration to short base-
emitter junctions at desired interconnections, or by other means. Abbreviated FPLA. Also known as programmable logic array.

THE GAL 16V8 (GENERIC ARRAY LOGIC)

The **Generic Array Logic** (also known as **GAL** and sometimes as gate array logic[1]) device was an innovation of the PAL and was invented by Lattice Semiconductor. The GAL was an improvement on the PAL because one device type was able to take the place of many PAL device types or could even have functionality not covered by the original range of PAL devices. Its primary benefit, however, was that it was eraseable and re-programmable, making prototyping and design changes easier for engineers.



THE ALTERA EPM7128S CPLD

MAX 7000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times