**Summary Assignment**

**Analog Multipliers**

In analog-signal processing the need often arises for a circuit that takes two analog inputs and produces an output proportional to their product. Such circuits are termed analog multipliers. Some types of analog multipliers include;

1. Emitter-coupled pair simple multiplier**;** The emitter-coupled pair, was shown to produce output currents that were related to the differential input voltage by;

Assuming (Vid/2VT­) << 1, then

IEE is bias current.

This shows that the emitter-coupled pair by itself can be used as a primitive multiplier.

* Two Quadrant restriction; With the addition of more circuitry, we can make IEE proportional to a second input signal.

The produced circuit functions as a multiplier under the assumption that Vid is small, and that Vi2 is greater than VBE(on). This means that the multiplier functions in only two quadrants of the Vid – Vi2 plane, and is termed a two-quadrant multiplier. Most practical multipliers allow four-quadrant operation.

1. Gilbert multiplier cells; The Gilbert multiplier cell, is a modification of the emitter-coupled cell, which allows four-quadrant multiplication. The Gilbert multiplier cell is the basis for most integrated-circuit balanced multiplier systems. The series connection of an emitter-coupled pair with two cross-coupled, emitter-coupled pairs produces a particularly useful transfer characteristic.

Substituting Ic1 and Ic2 into Ic3, Ic4, Ic5 and Ic6 we have;

Therefore,

Gilbert Cell Applications:

The dc transfer characteristic is the product of the hyperbolic tangent of the two input voltages. There are three main application of Gilbert cell depending of the V1 and V2 range:

* V1 < VT and V2 < VT then tanh(V1,2/ 2VT) ~ V1,2/ 2VT and the circuit acts as a multiplier
* V1 > VT and V2 < VT or V1 < VT and V2 > VT then the circuit acts as a modulator
* V1 > VT and V2 > VT ­then all six transistors are non-saturating switches and acts in phase detector mode.

**Phased Locked Loop Circuits**

A PLL is a feedback system that includes a VCO, phase detector, and low pass filter within its loop. Its purpose is to force the VCO to replicate and track the frequency and phase at the input when in lock. It is a control system allowing one oscillator to track with another. It is possible to have a phase offset between input and output, but when locked, the frequencies must exactly track.

The PLL output can be taken from either Vcont, the filtered (almost DC) VCO control voltage, or from the output of the VCO depending on the application. The former provides a baseband output that tracks the phase variation at the input. The VCO output can be used as a local oscillator or to generate a clock signal for a digital system. Either phase or frequency can be used as the input or output variables. Phase and frequency are interrelated by;

**Applications;** There are many applications for the PLL, but we will study the following:

* Clock generation
* Frequency synthesizer
* Clock recovery in a serial data link.

**Phase detector**

 This compares the phase at each input and generates an error signal, Ve(t), proportional to the phase difference between the two inputs. KD is the gain of the phase detector (V/rad).

An analog multiplier can also be used as a phase4 detector. Recall that the multiplier takes the product of two inputs. Ve(t)= A(t)B(t). Then if,

Then,

Since the two inputs are at the same frequency when the loop is locked, we have one output at twice the input frequency and an output proportional to the cosine of the phase difference. The doubled frequency component must be removed by the low-pass loop filter. Any phase difference then shows up as the control voltage to the VCO, a DC or slowly varying AC signal after filtering.

**VCO**

In PLL applications, the VCO is treated as a linear, time-invariant system. Excess phase of the VCO is the system output. The VCO oscillates at an angular frequency, ωout. Its frequency is set to a nominal ω0 when the control voltage is zero. Frequency is assumed to be linearly proportional to the control voltage with a gain coefficient KO or KVCO (rad/s/v).

**PLL Dynamic Response**

To see how the PLL works, suppose that we introduce a phase step at the input at t = t1

A phase step shows that initial and final frequencies must be the same, but a temporary change in frequency is required to shift the phase by φ1. Vcont is proportional to output frequency.

After settling, all parameters are as before since the initial and final frequencies are the same. This shows that Vcont(t) can be used to monitor the dynamic phase response of the PLL.

Now for a frequency step,

The frequency step will cause the phase difference to grow with time since a frequency step is a phase ramp. This in turn causes the control voltage, Vcont, to increase, moving the VCO frequency up to catch up with the input reference signal. In this case, we have a permanent change in ωout since a higher Vcont is required to sustain a higher ωout. If the frequency step is too large, the PLL will lose lock.

**Lock Range**

This is a range of input signal frequencies over which the loop remains locked once it has captured the input signal. This can be limited either by the phase detector or the VCO frequency range.

1. If limited by the phase detector; 0 < φ < π is the active range where lock can be maintained. For the phase detector type shown (Gilbert multiplier), the voltage vs. phase slope reverses outside this range. Thus the frequency would change in the opposite direction to that required to maintain the locked condition. When the phase detector output voltage is applied through the loop filter to the VCO,

Where KV = KOKD, the product of the phase detector and VCO gains.

1. The lock range could also be limited by the tuning range of the VCO. Oscillator tuning range is limited by capacitance ratios or current ratios and is finite. In many cases, the VCO can set the maximum lock range.

**PLL as a Feedback System;**

* Loop gain:

The loop gain can also be described as the polynomial below

* Transfer function:
* Order: The order of the polynomial in the denominator.
* Type: (n) the exponent of the s factor in the denominator.
* Phase Error:
* Steady State Error:

This is the Laplace Transform final value theorem.

For a PLL with feedback of 1, input and output frequencies are identical. The input and output phase should track one another, but there may be fixed offset depending on the phase detector implementation.

Transfer function with feedback of 1:

And the phase error function is:

 Open loop gain T(s):

We know that the phase detector will be producing an output equal to or at twice the carrier frequency, thus some low pass filtering will be needed. Let’s start with a simple RC lowpass network. ω1 = 1/RC. Thus, the filter transfer function is a simple lowpass.

Then T(s) becomes second order, type 1:

**Root Locus**: Since there are no zeros, the root locus represents the roots of the denominator of the closed loop transfer function. Set 1 + T(s) = 0 and solve for s as a function of KV.

We see that as KV is increased, the roots approach one another then become complex conjugates. We can have a very underdamped response when ω1 << KV. From the inverse Laplace transform of the complex conjugate pole pair there is an exponentially decaying term determined by the real part of the roots that shows how long it takes the system to settle after a phase or frequency step and a ringing frequency dictated by the imaginary part of the pole pair. When ω1 << KV, we have a high ringing frequency and a long settling time, characteristic of a system that is not very useful. Introducing a natural frequency and damping factor we have 1 + T(s) as

Where,

1 + T(s) can be written as,

This form allows you to use standard equations and normalized plots to describe the frequency and transient response of the system. As we saw with the other ways of representing the frequency response of the system, a large KV, which we like for reducing phase error, leads to a small ζ, which is bad for stability and settling time. So, it is clear that we need a better transfer function that gives us more flexibility in determining the bandwidth of the filter and the stability of the system. Add a zero to the loop filter transfer function to manipulate the root locus and improve stability.

Adding a resistor to the lowpass loop filter contributes a zero to its transfer function.

Where,

Thus, the zero frequency is always higher than the pole frequency. Small values of ω1 can be used for narrower filter bandwidth, or higher KV values can be used for lower phase error without sacrificing phase margin.

The transfer function for the pole-zero loop filter will be

The denominator is of the form 1 + T(s). We can also extract ωn and ζ from the closed loop transfer function since the denominator is in one of the standard forms.

Then solving for s, the poles are,

We see that ωn is the same as with the simple RC filter, but the damping factor has an added term. The first term is quite small in most cases, but the second term can be made large by increasing KV or reducing ω2. We still have a type 1 system, but we have an added term that we can use to improve stability, the zero frequency. Note that the zero is in the forward path and therefore shows up in the closed loop transfer function. It will affect the frequency and transient response.

**Loop Filter-OpAmp**

An op amp can be used to form a filter that includes a pole at s = 0 and a finite zero. A basic op-amp loop filter circuit would have the open loop transfer function F(s) as,

**Synthesizer PLL:** We will now add the divider 1/N to the feedback path. This architecture is called an “integer-N” synthesizer**.** We can calculate loop gain, T(s):

* We see that loop gain is reduced by a factor of N
* In most cases N is not constant
* KV = KDK­O varies with frequency according to the choice of N

Using the F(s) determined for the opamp pole-zero loop filter:

Where, ω1 = 1/R1C and ω2 = 1/R2C

We can now determine how the natural frequency and damping are affected by N:

**Phase Frequency Detector**

The phase-frequency detector is widely used in frequency synthesizers. As opposed to the XOR phase detector, this one produces two outputs: QA and QB, or as is customary, UP and DOWN respectively. The phase detector has a much larger phase range (4π) of operation, and it will produce an output that drives the frequency in the right direction when it is out of lock. It also has zero offset when the phases are aligned and is insensitive to the duty cycle of the inputs since edge-triggered flip-flops are used.

When the phases coincide, both outputs produce minimum width pulses. When there is a phase or frequency error, the width of the UP or DOWN pulses increases. When integrated by the loop filter, this causes the control voltage of the VCO to move toward the locked condition of equal frequency and phase. Because both outputs must be combined to obtain the desired output, the loop filter must be modified for differential inputs. F(s) is the same as that of the single ended version.

**Charge Pump Loop Filter**

An alternative loop filter implementation called the charge pump is widely used for many applications. It is very convenient to implement in CMOS.

* The PFD output produces UP (QA) and DOWN (QB) pulses whose width is proportional to the phase error.
* Charge pump current sources I1 and I2 must produce exactly equal currents. They charge and discharge the capacitor, CP, in discrete steps.
* If there is a static phase error ∆φ at the PFD input, the capacitor, C, will be charged indefinitely – therefore, the DC gain is infinite: an ideal integrator. So, we expect to have zero static phase error. This is unlike the type 1 loop which gave ∆φ = ∆ω/KV steady state phase error.
* The CP PLL will detect small phase errors and correct them as long as the frequency of the phase error (jitter frequency) is within the loop 3 dB bandwidth. This phase comparison occurs on every cycle.

To illustrate how the charge pump works and how it might be analyzed in a linearized model, we assume that I1 = I2 = IP and that a phase step ∆φ occurs at t = 0. ∆φ = φ0 u(t)

QA produces pulses that are of width

IP charges CP by

in every period. We can approximate this as a linear ramp with slope

Thus, the output voltage (step response) from the charge pump can be described by

The derivative of the step response with respect to time is the impulse response, taking the laplace transform we can determine the frequency domain transfer function as,

The loop gain function T(s), for the CP PLL is therefore,

We see that it has a factor of s2 in the denominator, thus it is a type 2 loop. But because of that we have a big problem, the phase margin is always zero. Therefore, we must add a zero to the loop filter transfer function to provide some phase lead to stabilize the PLL.

To determine T(s) for this case, we want to calculate Vout(s)/∆φ again, adding the resistor to the charge pump filter. To find the frequency response of the input current, we note that,

where Z(s) is the complex impedance. So, the current source can be modeled as:

Now, let’s use this to modify H(s) for the series RC loop filter. To do this, just replace the impedance 1/sCP with Z(s) = RP + 1/sCP.

The loop gain T(s) is therefore

We see that a zero at ω = 1/RPCP has been added to the transfer function. This provides the necessary phase lead to achieve stability. A frequency divider can be placed in the feedback path if the output frequency is to be multiplied by the PLL. This gives

This added divider would be needed in a frequency synthesizer application or clock multiplier application. T(s) would then become

Defining KV = IPKVCO/2πCP and zero frequency ωZ= 1/RPCP we can derive the closed loop transfer function as

Having put this in one of the standard forms, we can extract ωn and ζ from the denominator.

We can see now with RP = 0, ζ = 0, therefore there is no phase margin and the system is unstable as expected. With added RP, the damping factor can be increased. Also note that stability will decrease with increasing N. Loop gain must be increased to compensate for this.

The pole locations are found at

**Closed Loop Frequency Response**

The closed loop frequency response can be evaluated from H(jω). The loop 3 dB bandwidth is important for noise considerations. It is determined by ωn and ζ, so bandwidth must be determined in conjunction with the overshoot and settling time specifications. We find again that the formula is different for the case with a forward path zeros as opposed to the feedback zero case.

We see that the frequency response is a low pass to φin. Thus, the phase noise of the reference source passes through the PLL and is filtered. Below the 3 dB frequency, we have little attenuation of input noise. Above, noise is reduced by 40 dB/decade. Also note that for ζ < 2, there is gain peaking. Actually there is always some gain peaking for the Type II CP PLL or the opamp filter PLL because the zero frequency is always less than the pole frequency in the strongly damped case.

**PLL Phase Noise**

We have considered how the bandwidth of the loop affects things like settling time and capture range. But it also plays a role in the PLL noise behavior. For frequency synthesis, we are interested in low phase noise. There are at least 2 main sources:

* reference noise – usually small since we frequently use a crystal oscillator
* VCO noise – often high. We hope that the PLL will suppress most of the noise, at least close to the carrier

The effect caused by each of these noise sources can be seen from the closed loop transfer functions.

Reference Noise:

This is a low pass transfer function. Its magnitude approaches N as s becomes small. Thus, reference phase noise is low pass filtered by the loop. Reference phase noise can be quite low when a crystal oscillator is used to generate the reference frequency.

VCO Noise:

This is a high pass closed loop transfer function. It approaches a magnitude of 1 as s becomes large. While LC VCOs can have low phase noise, they generally have smaller tuning range. RC or ring oscillator VCOs can be built with very wide tuning range but poor phase noise. The PLL can be used to clean up the VCO phase noise within the loop bandwidth.