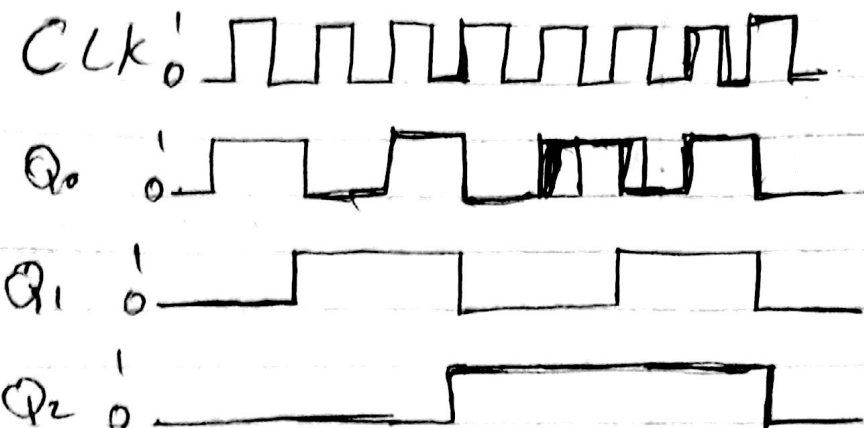
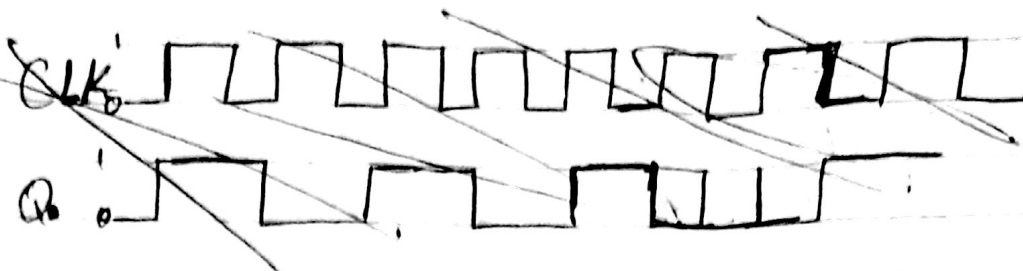
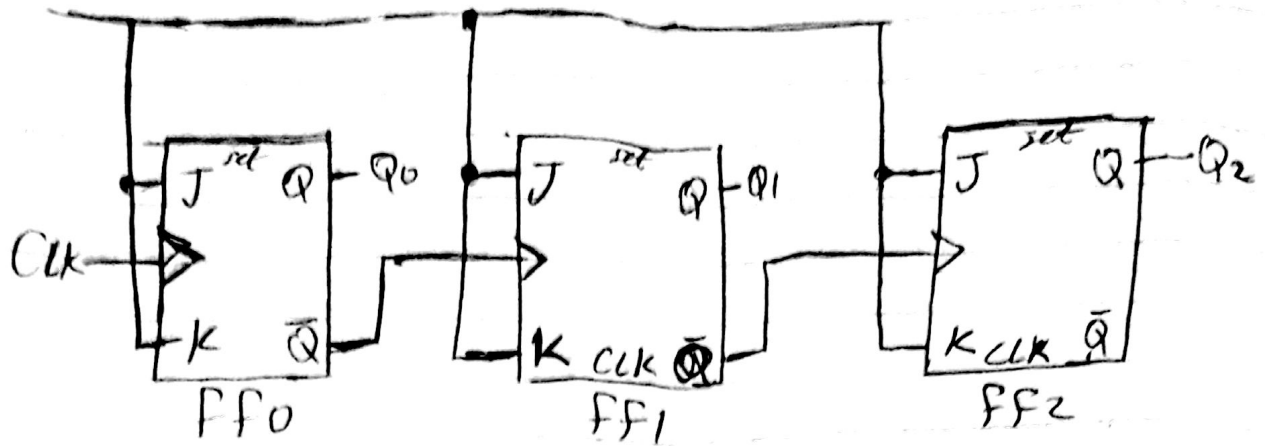


# A 3-Bit Asynchronous Counter



Timing Diagram

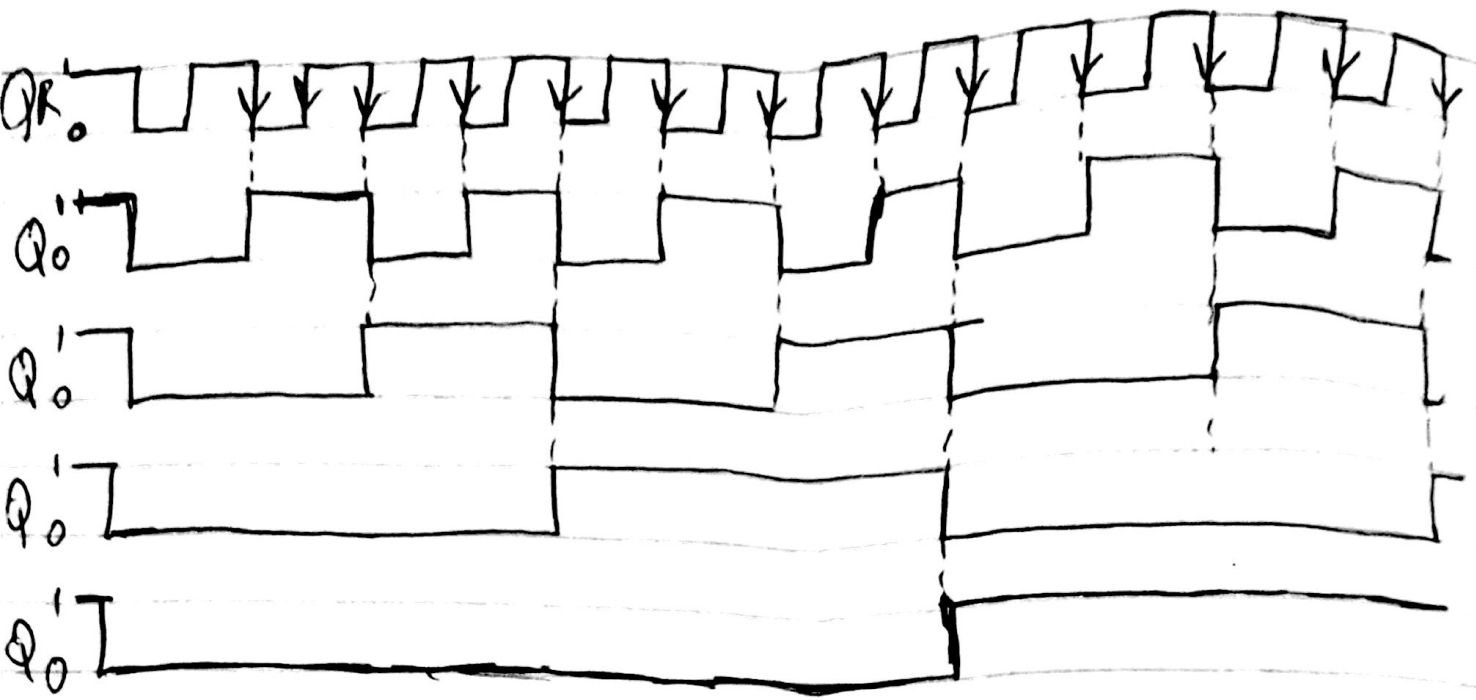
State	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Truth table

# BINARY COUNTING SYSTEM

$2^3$	$2^2$	$2^1$	$2^0$	
$Q_3$	$Q_2$	$Q_1$	$Q_0$	
0	0	0	0	Before applying clock pulse
0	0	0	1	After pulse 1
0	0	1	0	After pulse 2
0	0	1	1	After pulse 3
0	1	0	0	After pulse 4
0	1	0	1	" " 5
0	1	1	0	" " 6
0	1	1	1	" " 7
1	0	0	0	After pulse 8
1	0	0	1	After pulse 9
1	0	1	0	" " 10
1	0	1	1	" " 11
1	1	0	0	" " 12
1	1	0	1	" " 13
1	1	1	0	" " 14
1	1	1	1	" " 15
0	0	0	0	After pulse 16 (returns to 0000)
0	0	0	1	After pulse 17
0	0	1	0	" " 18
0	0	1	1	" " 19

0000  
0000



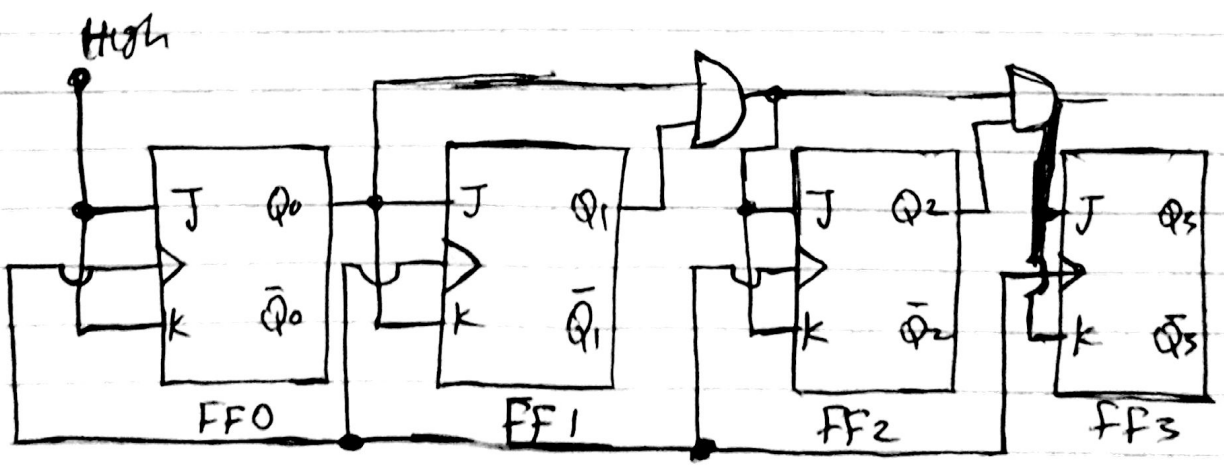
Timing diagram showing frequency division

- 2) i) MOD number =  $2^6 = 64$   
 ii) Frequency at the last flip flop =  $\frac{\text{Input Clock Freq.}}{\text{MOD number}}$   
 $\Rightarrow$  Frequency at  $Q_5 = 1/64 \text{ MHz} = 15625 \text{ kHz}$

iii) The counter will count from 000000 to 111111 (total of 64 states)

iv) Since it is a MOD 64 counter, every 64 pulses will bring the counter back to its initial state. Therefore, after 128 pulses, the counter is back to 000000 and after the 129th pulse, it brings the counter to 000001 state

### A 4-BIT BINARY COUNTER



### JK Truth table

J	k	Q
0	0	NO change
0	1	Reset (0)
1	0	set (1)
1	1	Toggle