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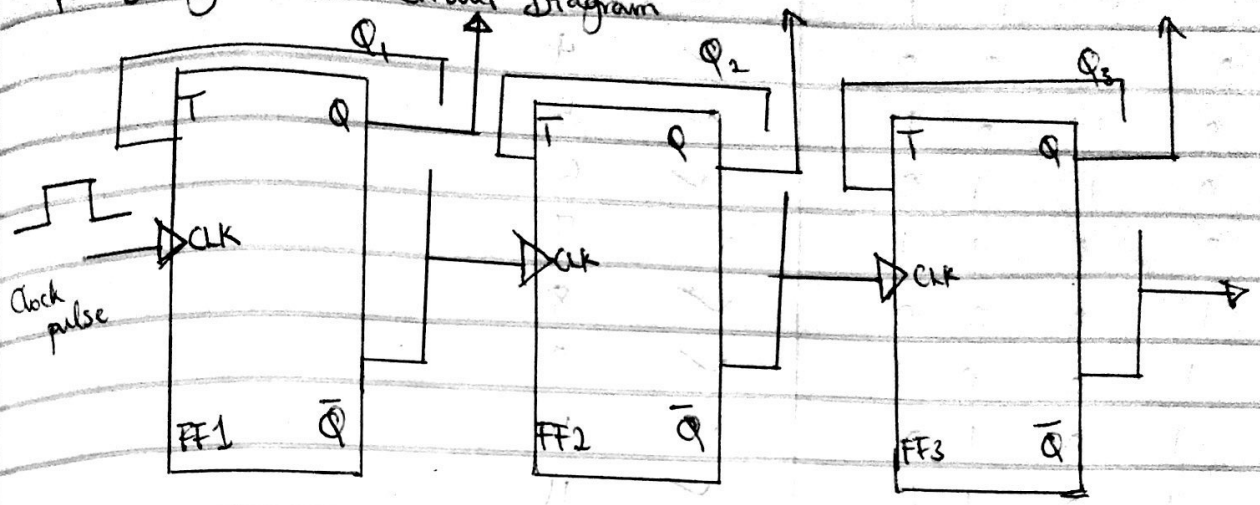
Matric No: 17/ENG02/033

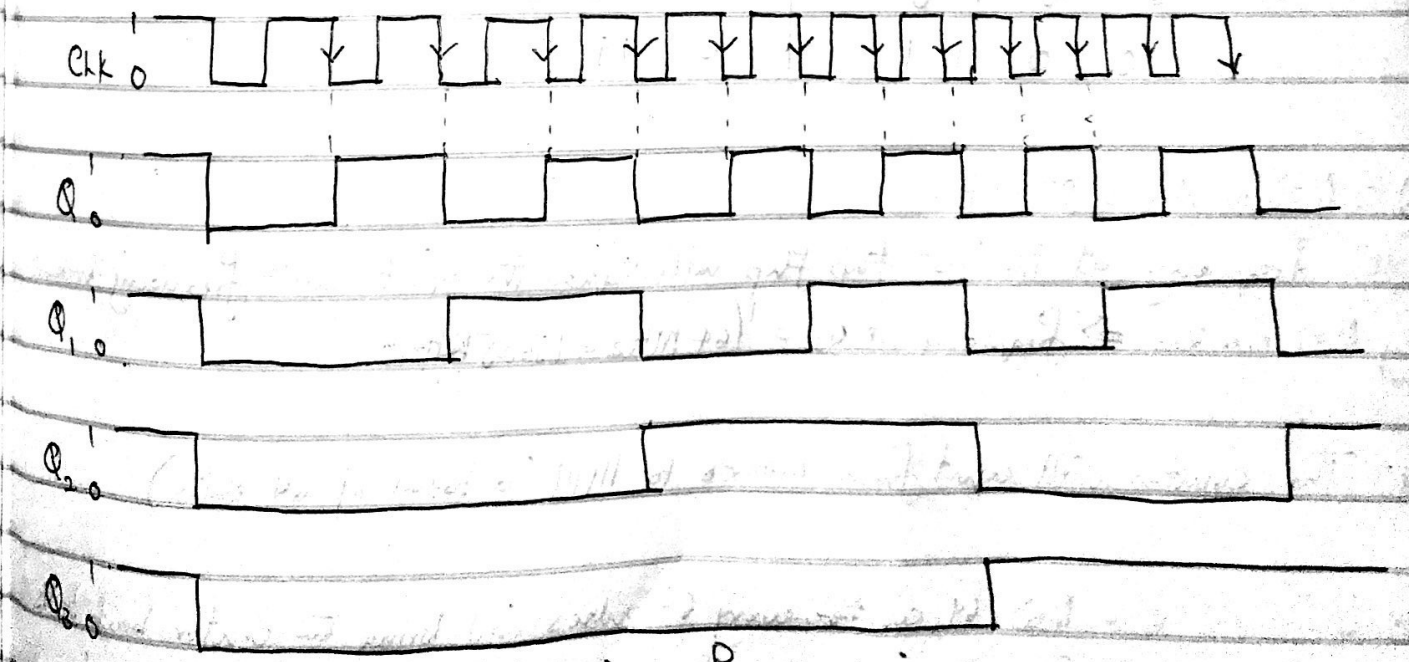
COE 512 Assignment

1. Binary Counter Circuit Diagram



J K truth table

J	K	Q
0	0	No change
0	1	Reset (0)
1	0	Set (1)
1	1	Toggle



Timing Diagram showing frequency divisi

Q_3	Q_2	Q_1	Q_0	
0	0	0	0	Before applying clock pulse
0	0	0	1	After pulse 1
0	0	1	0	✓ 2
0	0	1	1	✓ 3
0	1	0	0	✓ 4
0	1	0	1	✓ 5
0	1	1	0	✓ 6
0	1	1	1	✓ 7
1	0	0	0	✓ 8
1	0	0	1	✓ 9
1	0	1	0	✓ 10
1	0	1	1	✓ 11
1	1	0	0	✓ 12
1	1	0	1	✓ 13
1	1	1	0	✓ 14
1	1	1	1	✓ 15
0	0	0	0	After pulse 16 (returns to 0)
0	0	0	1	✓ 17
0	0	1	0	✓ 18
0	0	1	1	✓ 19

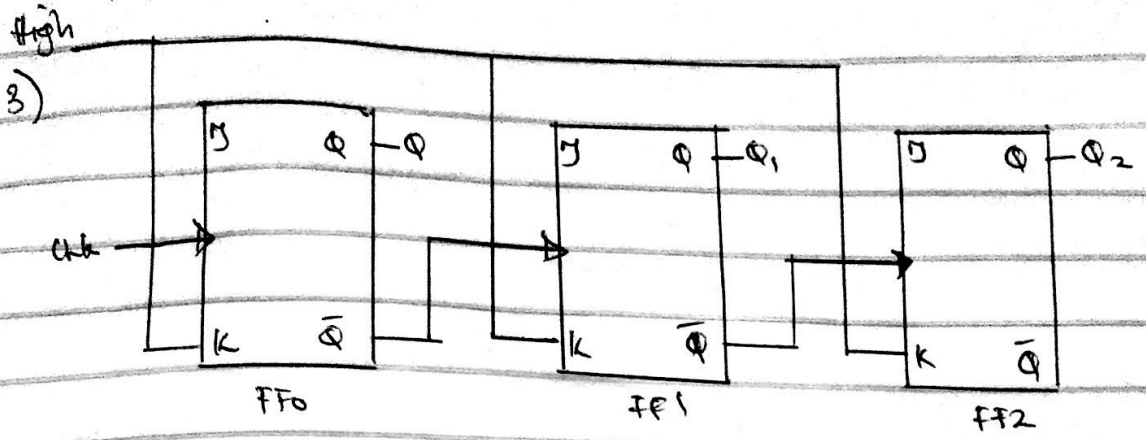
2) (a) MOD number $= 2^6 = 64$

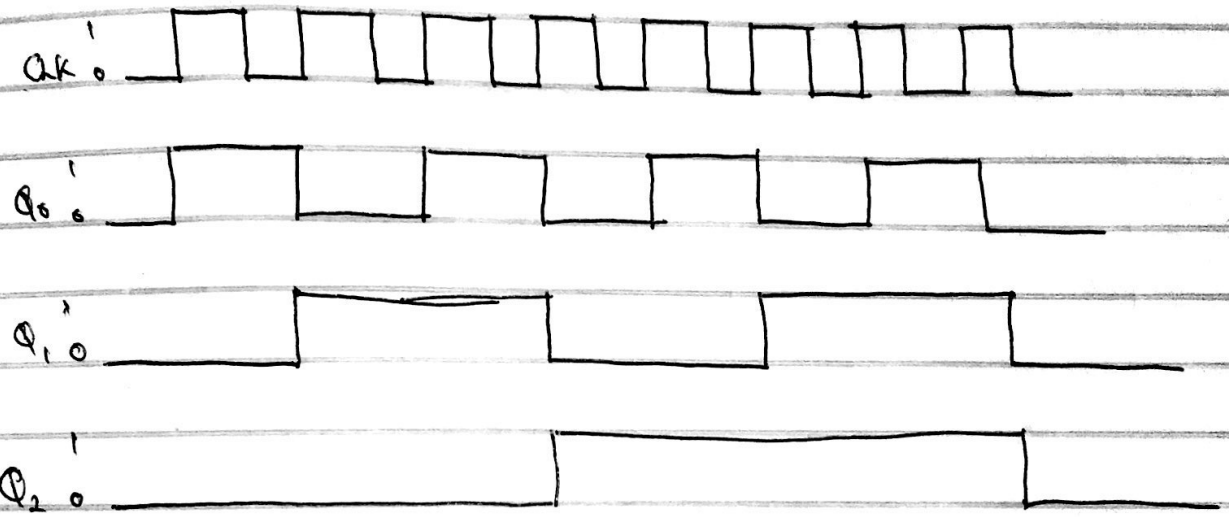
(b) Frequency at the last flip flop will equal the input clock frequency divided by MOD number $\Rightarrow$ frequency at $Q_5 = 1/64\ MHz = 15625\ kHz$.

(c) The counter will count from 000000 to 111111 (a total of 64 states)

(d) Since it is a MOD-64 counter, every 64 pulses will bring the counter back to its initial state. Therefore after 128 pulses, the counter is back to 000000 and after the 129th pulse, A brings the counter to 000001 state.

3)





State	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1