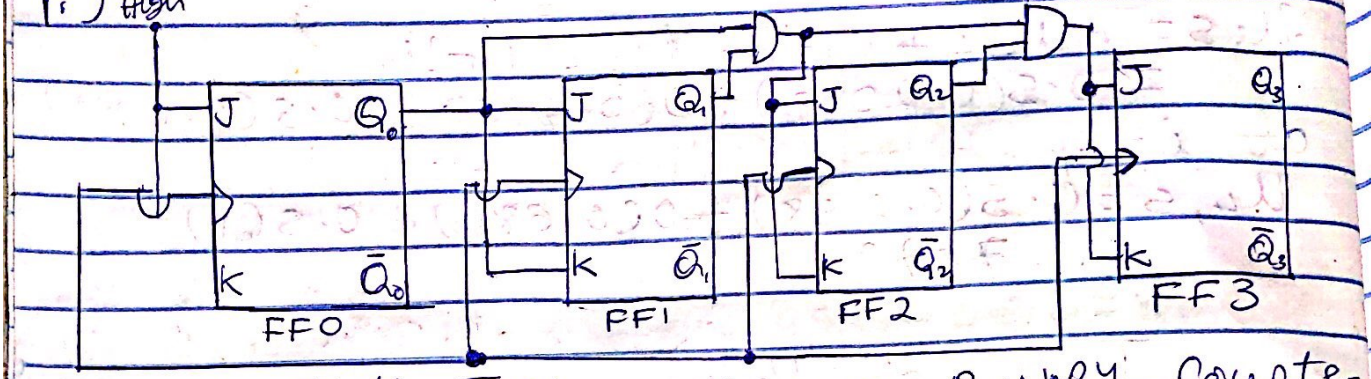
Nasir-Ameen Nasir
17/ENG02/045 Computer Engineering

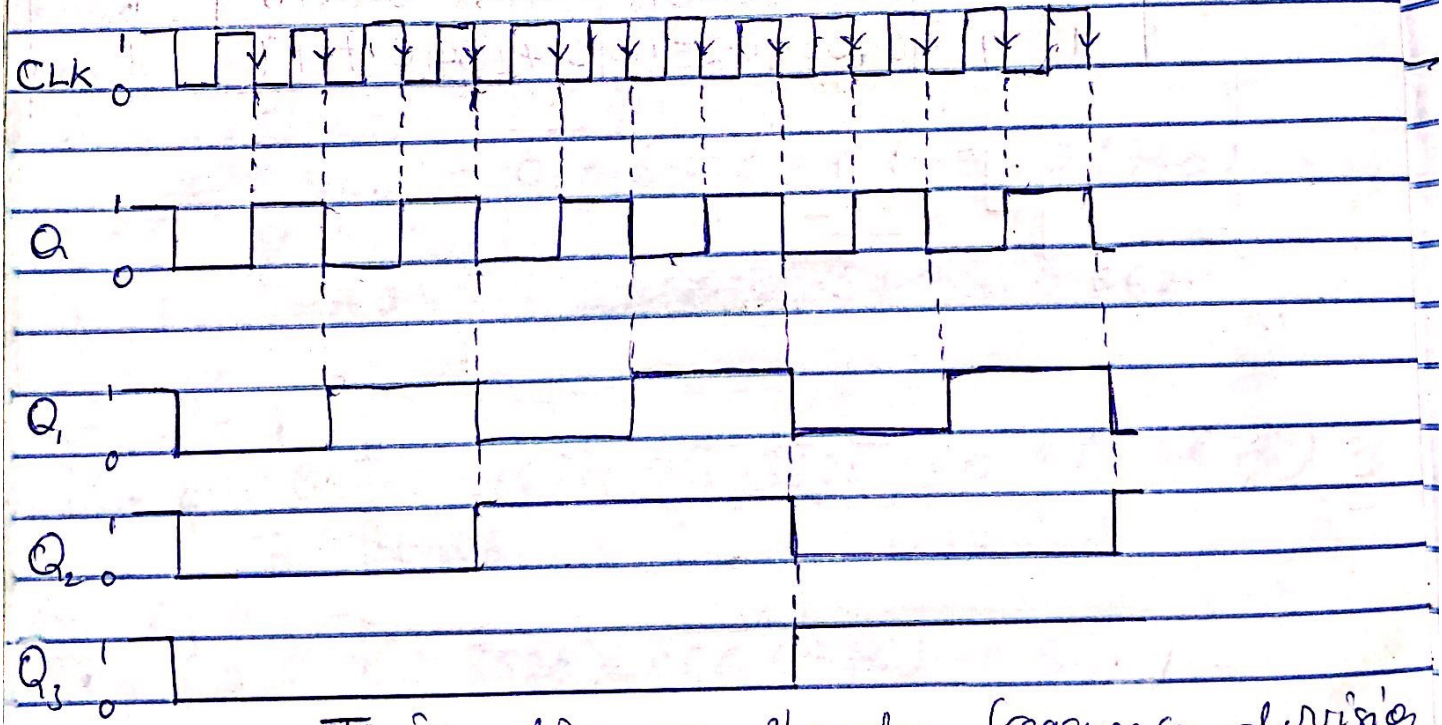
1.) High



4 BIT BINARY Counter

J K Truth Table

J	K	Q
0	0	No Change
0	1	Reset (0)
1	0	Set (1)
1	1	Toggle



Timing diagram showing frequency division

Binary Counting System

2^4 Q_3	2^3 Q_2	2^2 Q_1	2^1 Q_0	
0	0	0	0	Before applying clock pulse
0	0	0	1	After pulse 1
0	0	1	0	After pulse 2
0	0	1	1	After pulse 3
0	1	0	0	After pulse 4
0	1	0	1	After pulse 5
0	1	1	0	After pulse 6
0	1	1	1	After pulse 7
1	0	0	0	After pulse 8
1	0	0	1	After pulse 9
1	0	1	0	After pulse 10
1	0	1	1	After pulse 11
1	1	0	0	After Pulse 12
1	1	0	1	After pulse 13
1	1	1	0	After pulse 14
1	1	1	1	After pulse 15
0	0	0	0	After pulse 16 (returns to 0000)
0	0	0	1	After pulse 17
0	0	1	0	After pulse 18
0	0	1	1	After pulse 19

2.) i.) MOD number = $2^6 = 64$

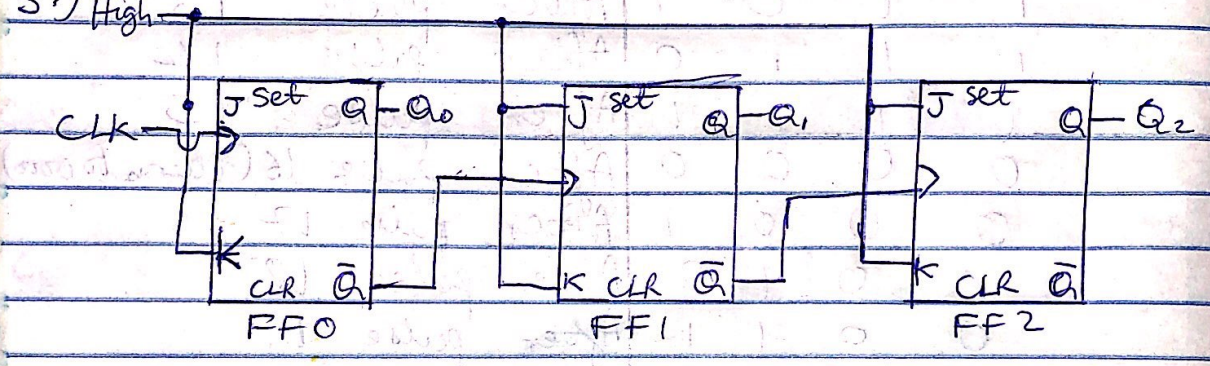
ii.) Frequency at the last flip flop will equal the input clock frequency divided by MOD number

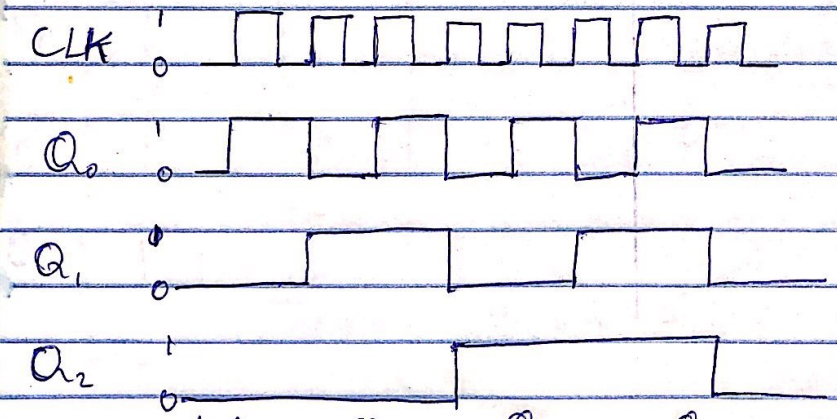
$\Rightarrow$ frequency at $Q_5 = \frac{1}{64}\ MHz = 15625\ KHz$

iii.) The counter will count from 000000 to 111111 (a total of 64 states)

iv.) Since it is a MOD 64 counter every 64 pulses will bring the counter back to its initial state. Therefore, after 128 pulses the counter is back to 000 000 and after the 129th pulse, it brings the counter to 000001 state.

3.)





Timing Diagram

State	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1