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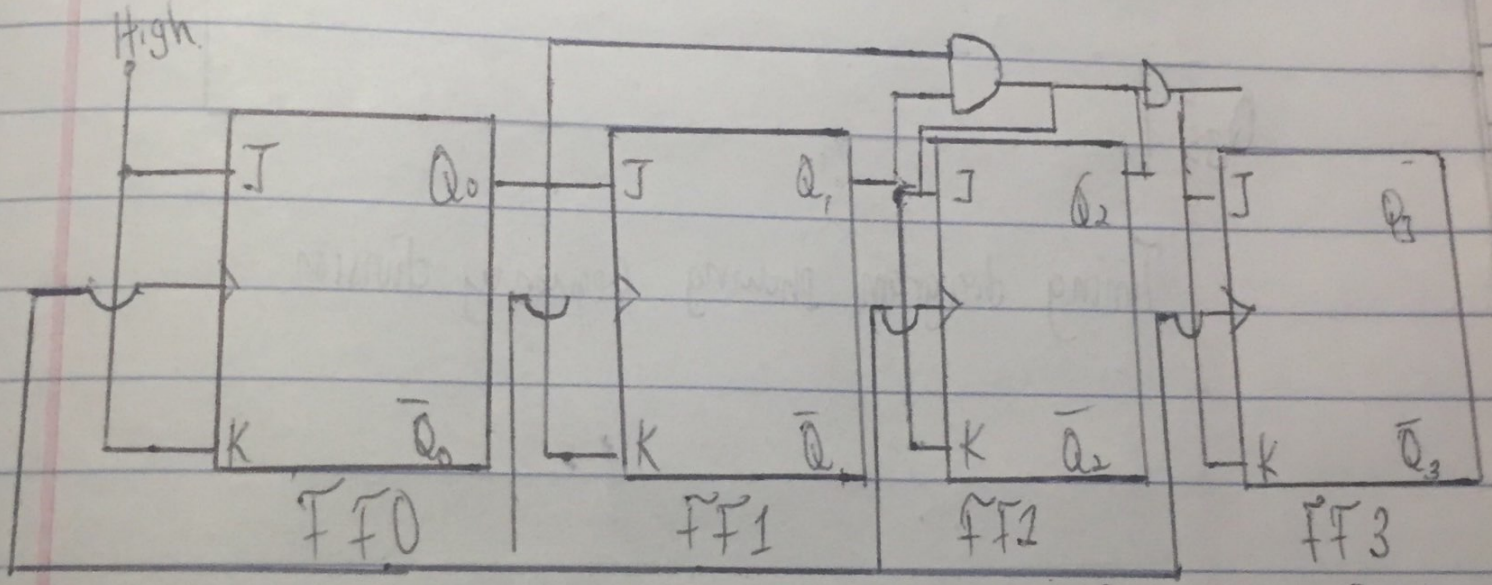
Matric Number: 17/MHS01/187

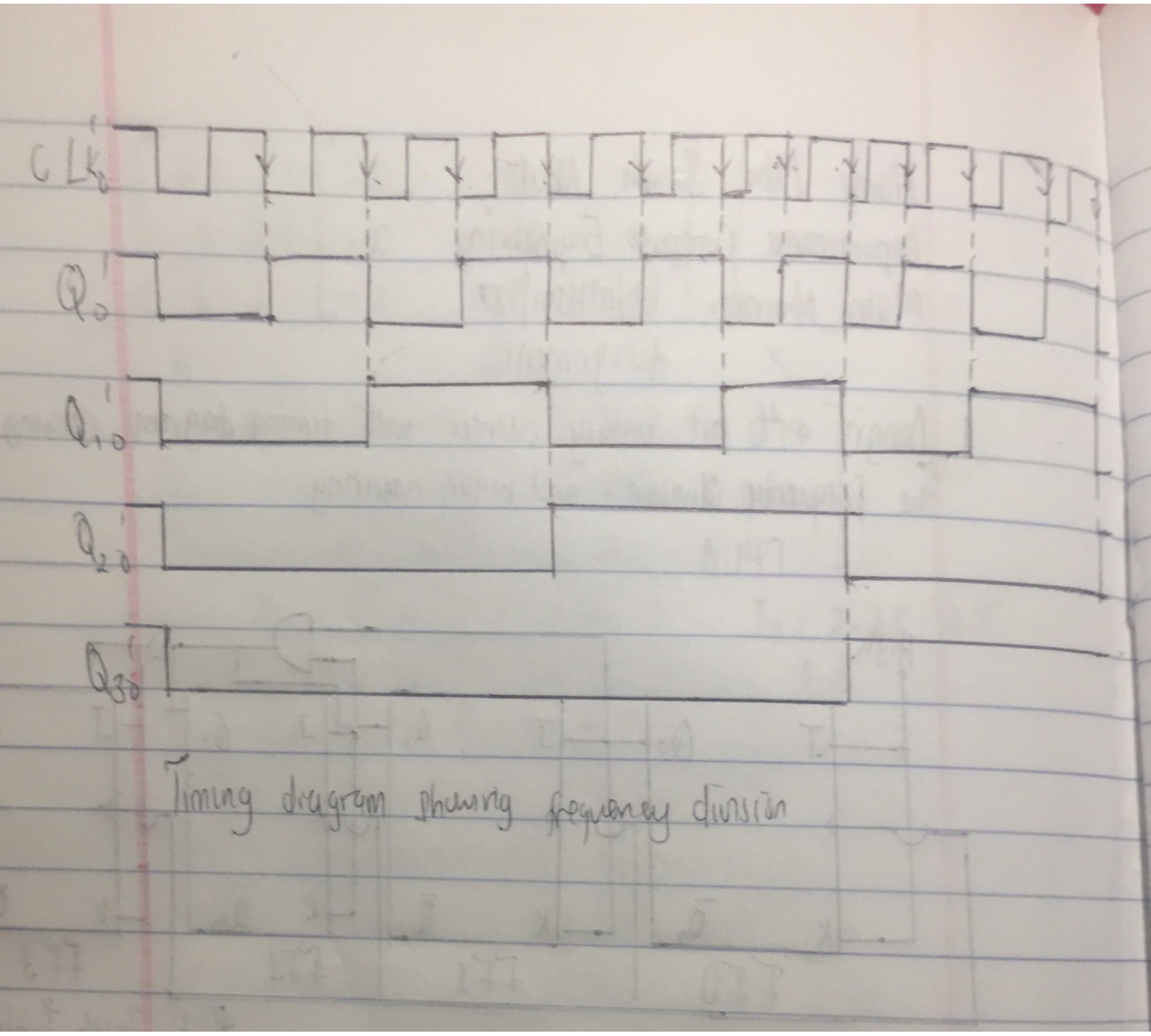
Assignment

1 Design a 4 bit binary counter with timing diagram showing the frequency division and binary counting



J K Truth Table

J	K	Q
0	0	No change
0	1	Reset (0)
1	0	Set (1)
1	1	Toggle



Timing diagram showing frequency division

BINARY COUNTING SYSTEM

Q_3 (2^3)	Q_2 (2^2)	Q_1 (2^1)	Q_0 (2^0)	
0	0	0	0	Before applying clock pulse
0	0	0	1	After pulse 1
0	0	1	0	✓ ✓ 2
0	0	1	1	✓ ✓ 3
0	1	0	0	✓ ✓ 4
0	1	0	1	✓ ✓ 5
0	1	1	0	✓ ✓ 6
0	1	1	1	✓ ✓ 7
1	0	0	0	✓ ✓ 8
1	0	0	1	✓ ✓ 9
1	0	1	0	✓ ✓ 10
1	0	1	1	✓ ✓ 11
1	1	0	0	✓ ✓ 12
1	1	0	1	✓ ✓ 13
1	1	1	0	✓ ✓ 14
1	1	1	1	✓ ✓ 15
0	0	0	0	After pulse 16 (Returns to 0000)
0	0	0	1	✓ ✓ 17
0	0	1	0	✓ ✓ 18
0	0	1	1	✓ ✓ 19

2; i MOD number = $2^6 = 64$

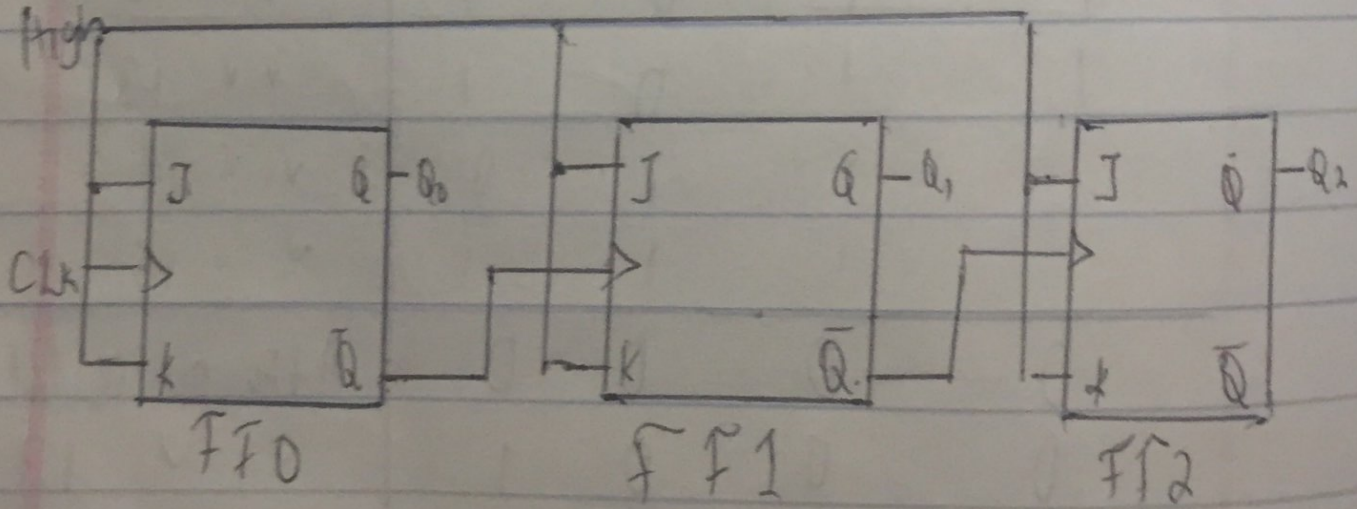
ii Frequency of the last flip flop will equal be the input clock frequency divided by MOD number

⇒ frequency of $CL_5 = \frac{1\ MHz}{64} = 15625\ KHz$

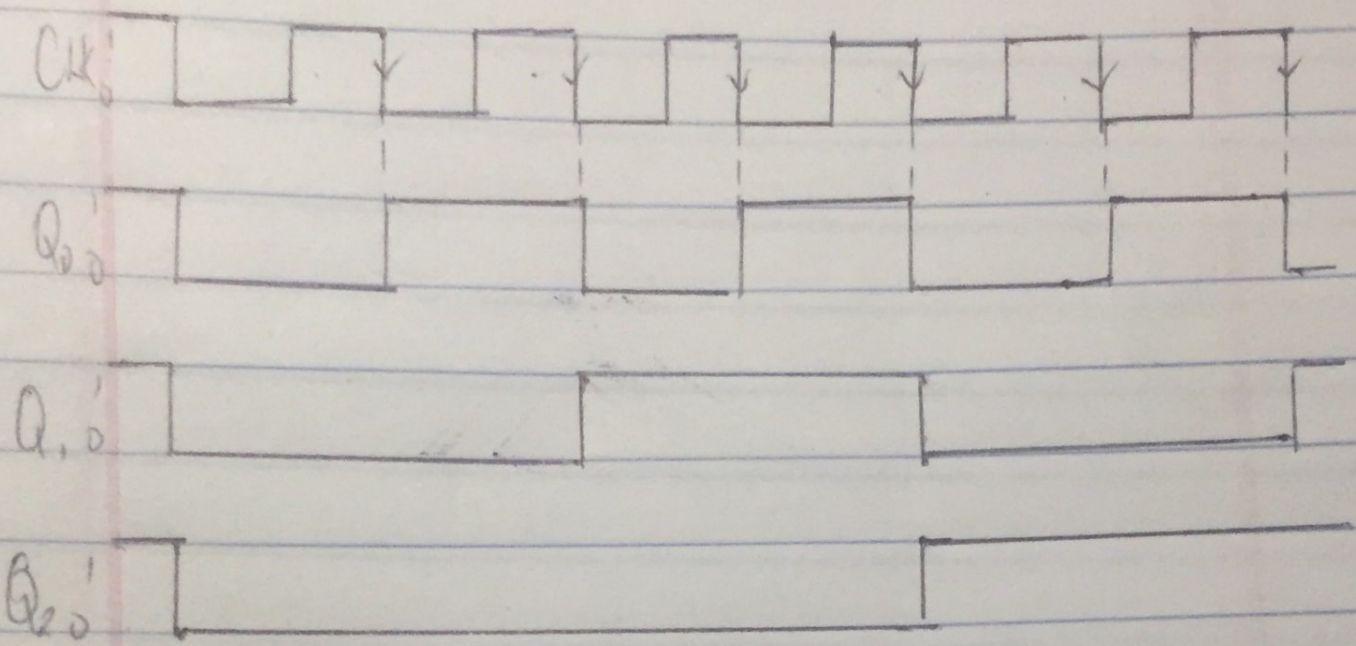
iii The counter will count from 000000 to 111111 (a total of 64 states)

iv Since it is a MOD-64 counter, every 64 pulses will bring the counter back to its initial state. Therefore, after 128 pulses, the counter is back to 000000 and after 129th pulse it brings the counter to output state

3 Design a 3 bit asynchronous counter



Timing Diagram



Truth Table

State	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1