IDE ALEXIUS AZIBANYE
17/ENG02/032
COMPUTER ENGINEERING.
SUBMITTED TO ENGR. ADIGUN LEVEL ADVISOR VIA LMS.

## ASSIGNMENT 1

Designing a 4-bit Binary Counter.


## ASSIGNMENT 2

a) A counter with six FFs $\left(Q_{0}, Q_{1}, Q_{2}, Q_{3}, Q_{4}, Q_{5}\right)$ will $=2^{6}$ which will equal to $=64$; There the Mod number of the Counter is MOD=16.
b) The Frequency of $Q_{5}$ is exactly one-half of the frequency of $Q_{4}$ therefore frequency will be $1 / 64^{\text {th }}$ of 1 Mhz .

c) The range counting states of the counter is ranging from $Q_{5}-Q_{0}(000000-011110$ ) $Q_{5}=M S B, Q_{0}=L S B$.
d) After the starting count of "000000", the 129 ${ }^{\text {th }}$ pulse will be "000001".

## ASSIGNMENT 3

- Designing a 3-bit Asynchronous (Ripple) Counter.


Timing Diagram

$Q_{2}=M S B, Q_{0}=L S B$.
RECYCLE TO 000.

