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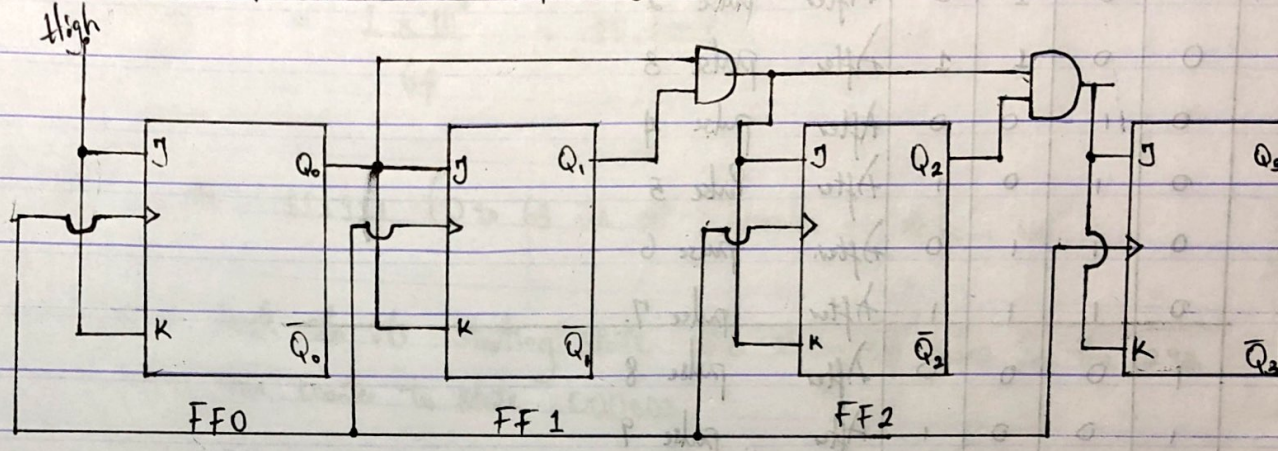
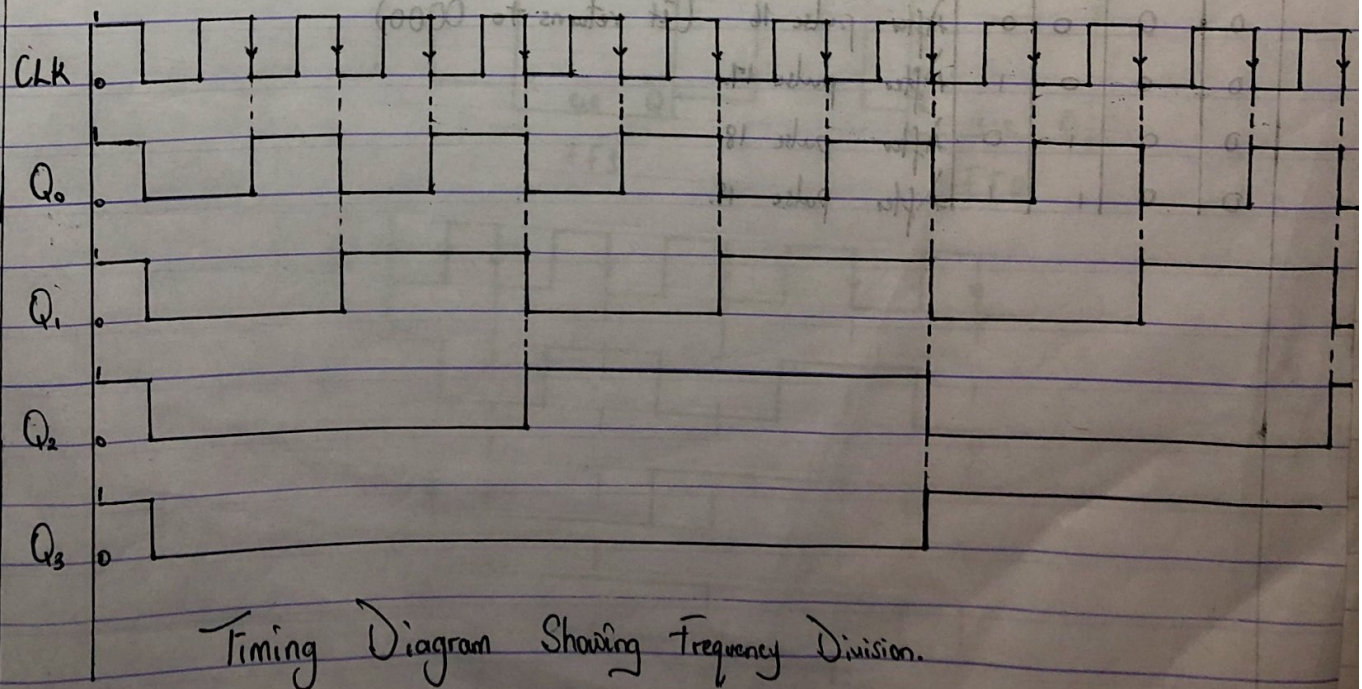
Assignment 1

A 4-BIT BINARY COUNTER.



JK Truth table.

J	K	Q
0	0	No change.
0	1	Reset (0)
1	0	Set (1)
1	1	Toggle.



Timing Diagram Showing Frequency Division.

BINARY COUNTING SYSTEM.

2^4 Q_3	2^3 Q_2	2^2 Q_1	2^1 Q_0	
0	0	0	0	Before applying clock pulse.
0	0	0	1	After pulse 1
0	0	1	0	After pulse 2
0	0	1	1	After pulse 3
0	1	0	0	After pulse 4
0	1	0	1	After Pulse 5
0	1	1	0	After pulse 6
0	1	1	1	After pulse 7.
1	0	0	0	After pulse 8
1	0	0	1	After pulse 9
1	0	1	0	After pulse 10
1	0	1	1	After pulse 11
1	1	0	0	After pulse 12.
1	1	0	1	After pulse 13.
1	1	1	0	After pulse 14.
1	1	1	1	After pulse 15.
0	0	0	0	After pulse 16 (it returns to 0000)
0	0	0	1	After pulse 17.
0	0	1	0	After pulse 18.
0	0	1	1	After pulse 19.

Assignment 2.

1. $Q_5, Q_4, Q_3, Q_2, Q_1, Q_0$ – MOD - 6 counter.

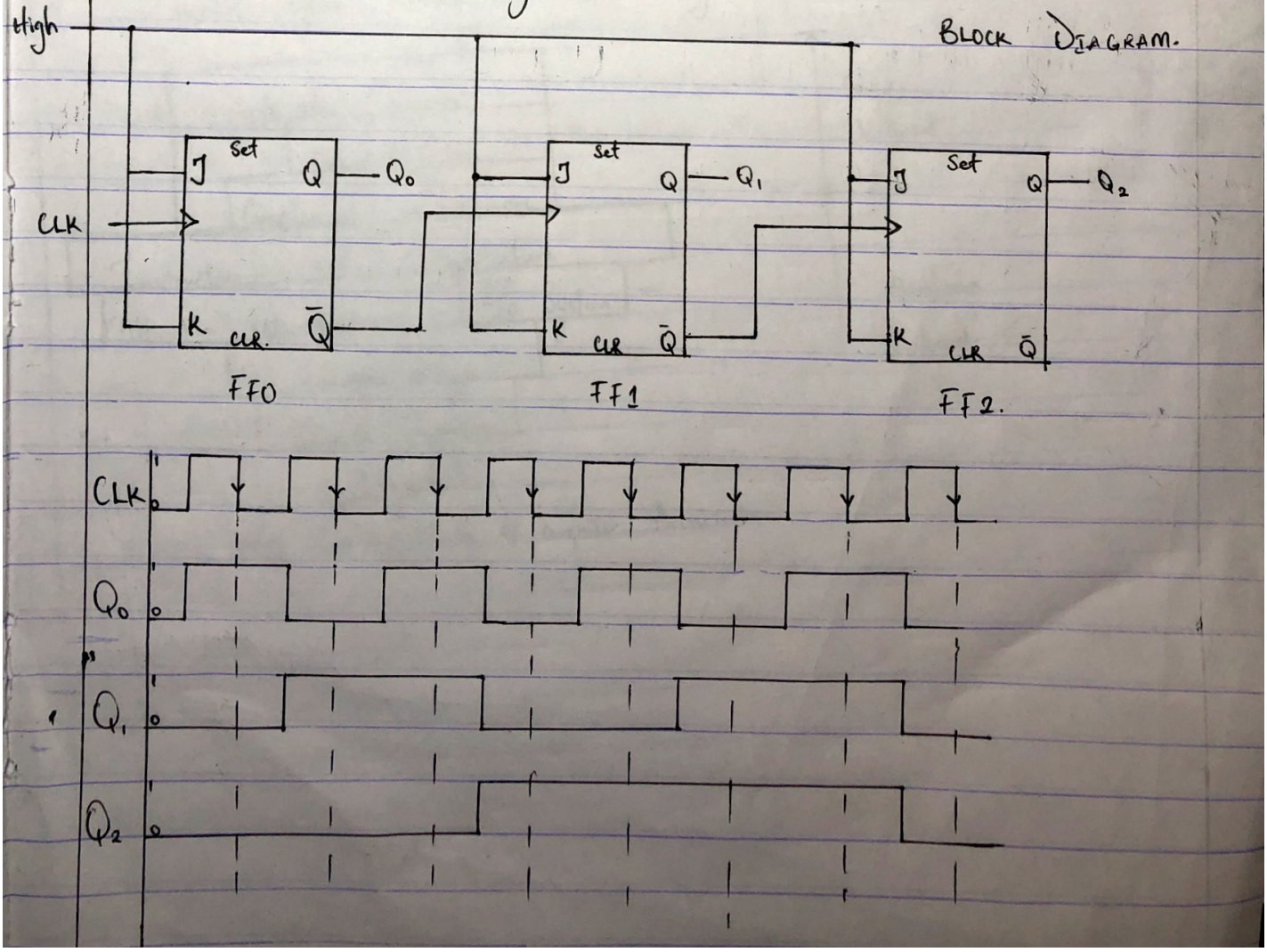
a. MOD - 64 counter (2^6)

b $F = \frac{1\,MHz}{64} = \frac{1 \times 10^3}{64} = 15.625\,KHz$

c 000000 to 111111 (0 to 63 i.e $2^6 - 1$) number of states = 64

d Counter will be back to its starting state after every 64 pulses. So the 129th pulse will bring the counter to state 000001.

2. A 3-Bit Asynchronous Counter.



TRUTH TABLE.

State	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1