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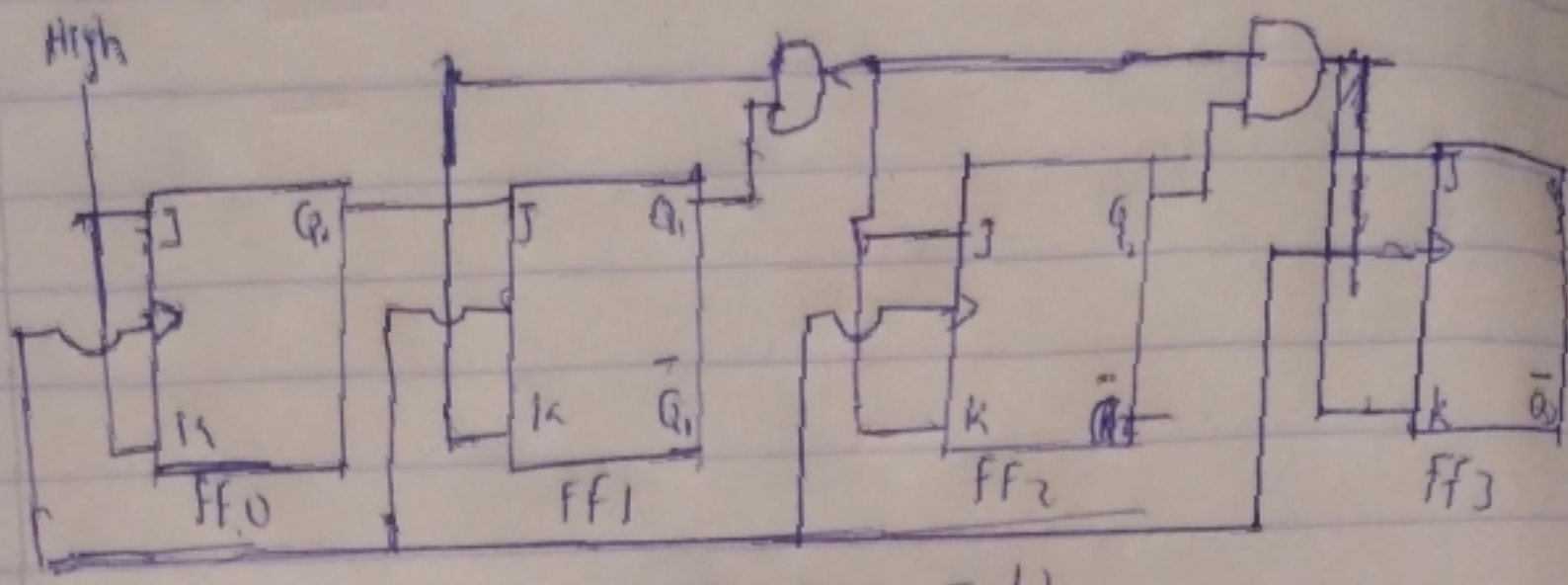
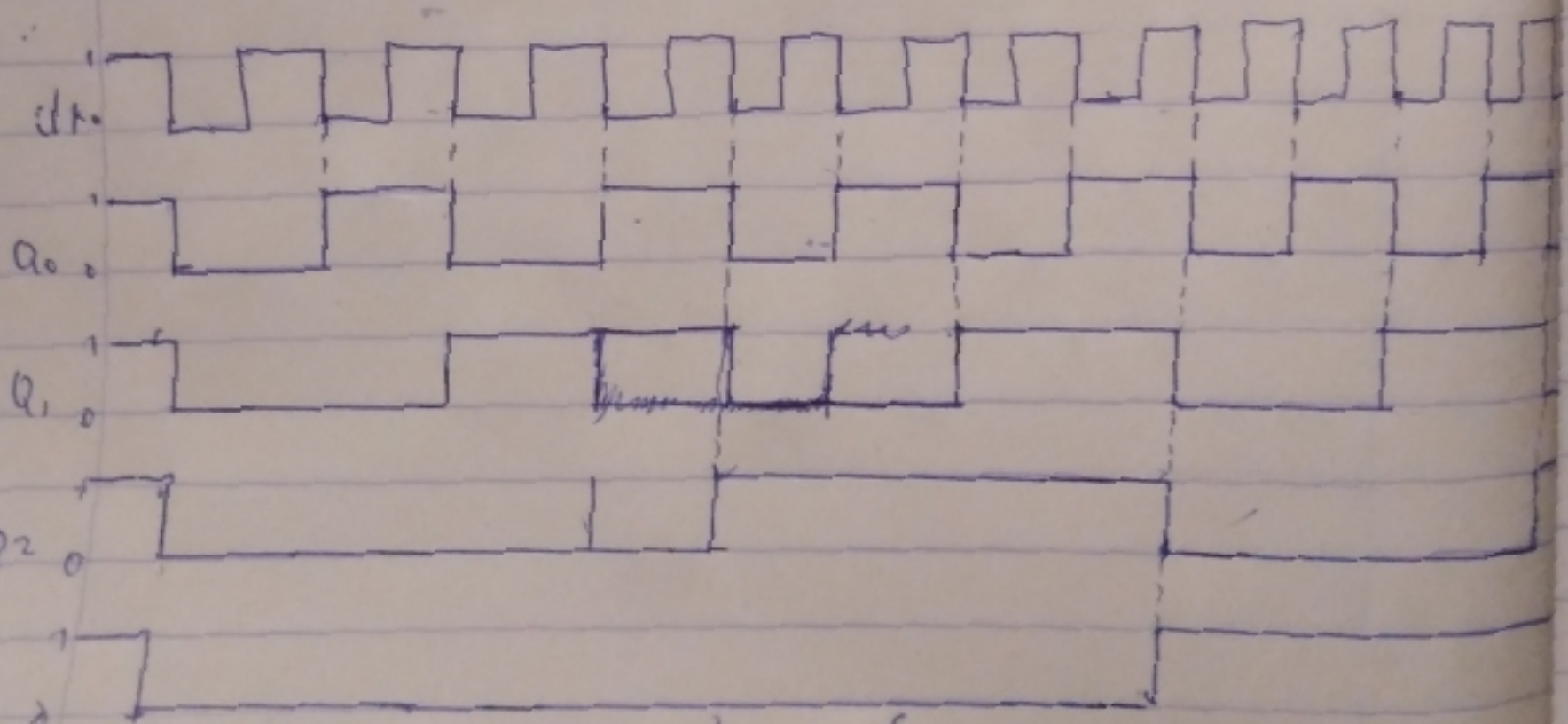
COE 312 ASSIGNMENT

A 4 Bit Binary Counter



J_K Time Table

J	K	Q
0	0	No change
0	1	Rest (0)
1	0	set (1)
1	1	Toggle



Timing diagram showing frequency division

Binary Counting System

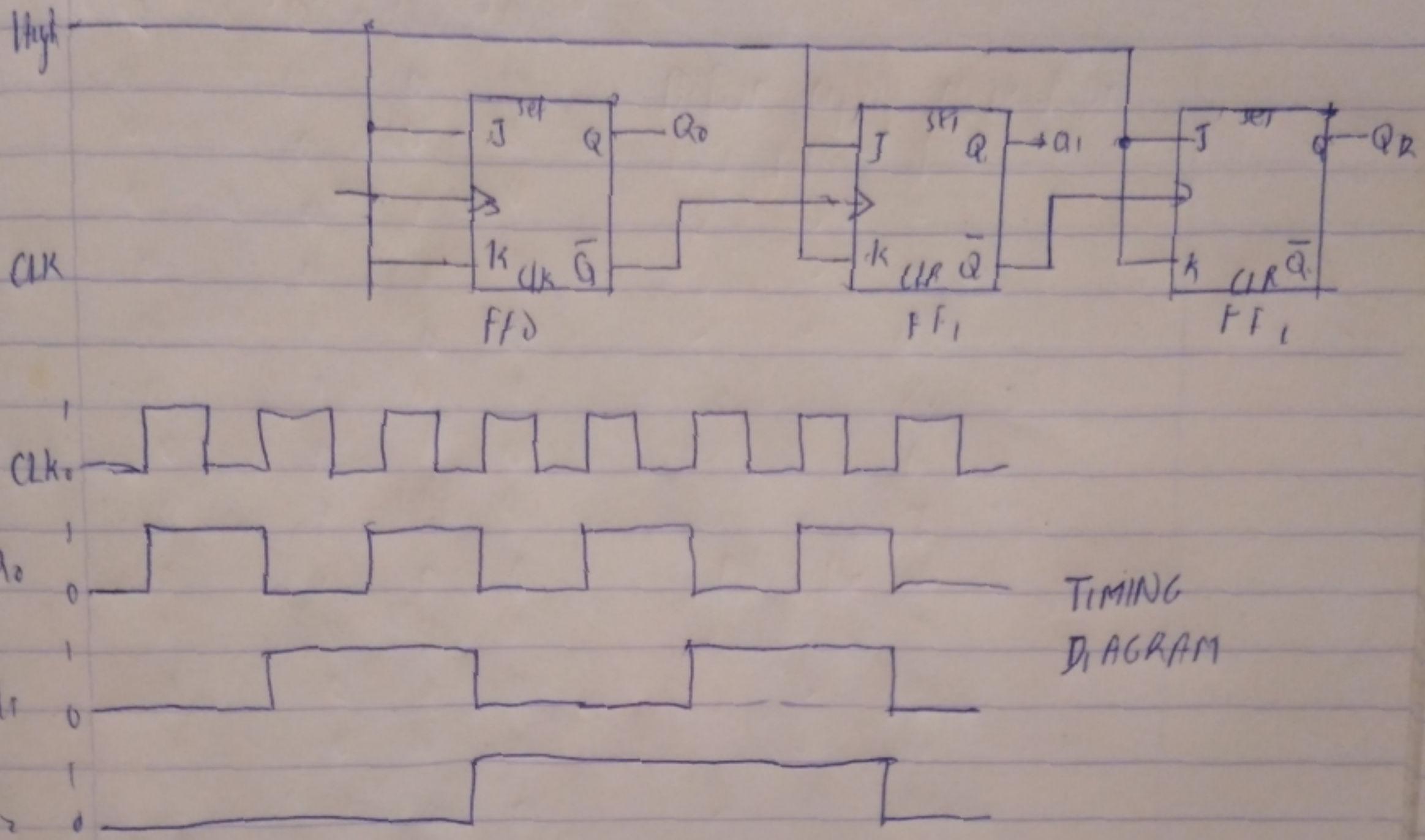
Q_3^{24}	Q_2^{2}	Q_1^{22}	Q_0^{2}		
0	0	0	0	Before apply Clock Pulse	
0	0	0	1	After Pulse 1	
0	0	1	0	/ /	2
0	0	1	1	/ /	3
0	1	0	0	/ /	4
0	1	0	1	/ /	5
0	1	1	0	/ /	6
0	1	1	1	/ /	7
1	0	0	0	After Pulse	8
1	0	0	1	/ /	9
1	0	1	0	/ /	10
1	0	1	1	/ /	11
1	1	0	0	/ /	12
1	1	0	1	/ /	13
1	1	1	0	/ /	14
1	1	1	1	/ /	15
0	0	0	0	After Pulse	16 [It returns to 00]
0	0	0	1	/ /	16
0	0	1	0	/ /	17
0	0	1	1	After Pulse	19

2. i MOD number $= 2^6 - 64$

ii Frequency at the base flip flop is equal the input Clock frequency divided by MOD number. $\Rightarrow$ frequency at Q_5 = $1/64$ MHz = 15625 kHz

iii The counter will count from 000 000 to 111 111. (a total of 64 stages)

iv Since it is a MOD. 64 counter, every 64 Process will bring the counter back to it's initial state, therefore, after 128 Pulse, the counter is back to 000000 and after 129th Pulse it brings the counter to 000001 state.



TIMING DIAGRAM

State	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

TRUTH TABLE