CPE 506 Assignment

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Matric No: 15/ENG02/003

1) $A(X_1 X_2 X_3 X_4) = \Sigma_m(3,7,8,9,11,15)$

$B(X_1 X_2 X_3 X_4) = \Sigma_m(3,4,5,7,10,14,15)$

$C(X_1 X_2 X_3 X_4) = \Sigma_m(1,5,7,11,15)$

Truth table below

| $X_1$ | $X_2$ | $X_3$ | $X_4$ | A | B | C |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Step 3: Find out the boolean representation of the outputs A, B and C

Output A:

| $X_3X_4$ \ $X_1X_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 1 |
| 01 | 0 | 0 | 0 | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 0 | 0 | 0 |

$$A = X_1\bar{X}_2\bar{X}_3 + X_3X_4$$

Output B:

| $X_3X_4$ \ $X_1X_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 0 | 0 |
| 01 | 0 | 1 | 0 | 0 |
| 11 | 1 | 1 | 1 | 0 |
| 10 | 0 | 0 | 1 | 1 |

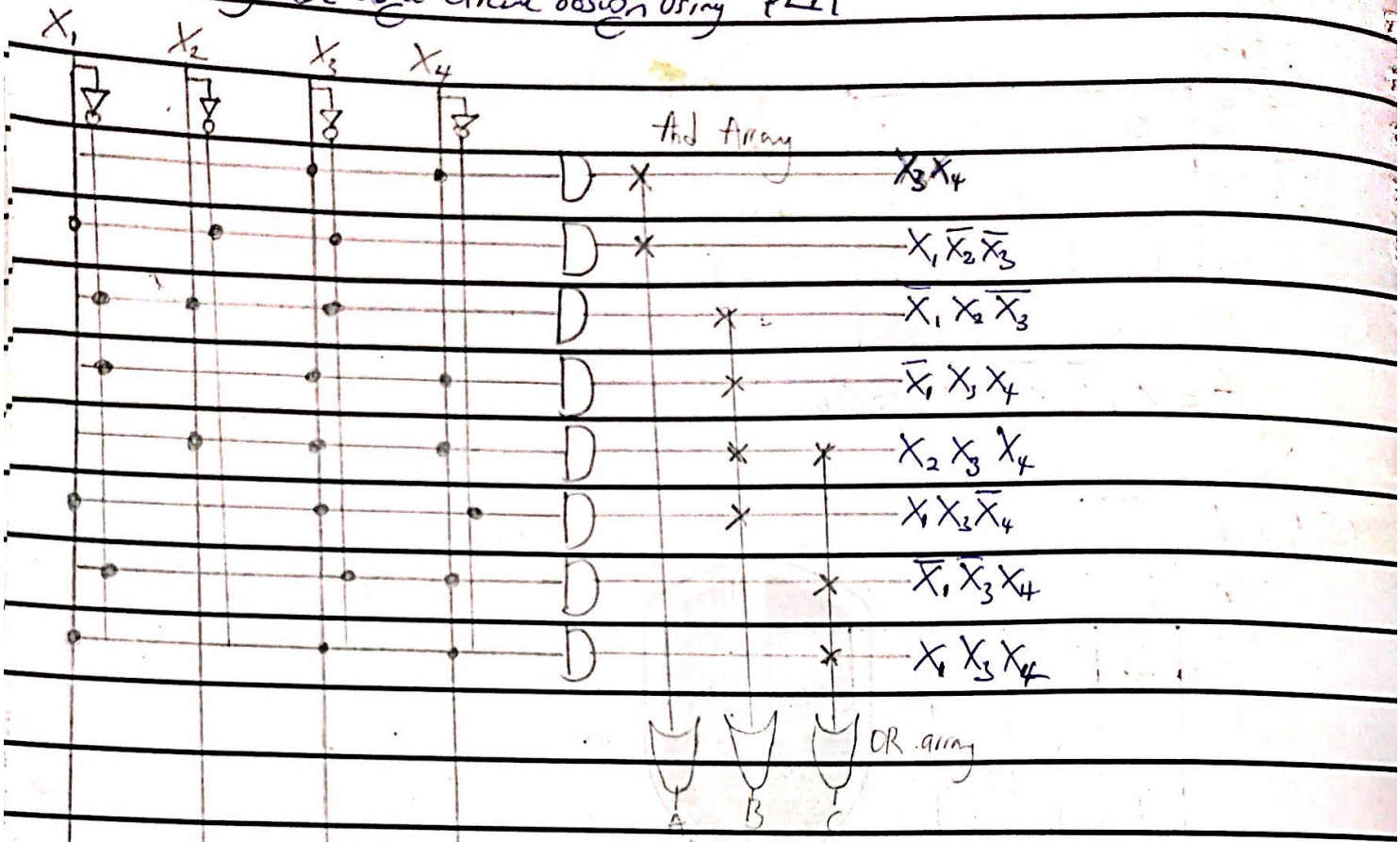
$$B = X_2X_3X_4 + X_1X_3\bar{X}_4 + \bar{X}_1X_3X_4 + \bar{X}_1X_2\bar{X}_3$$

Output C:

| $X_3X_4$ \ $X_1X_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 |
| 01 | 1 | 1 | 0 | 0 |
| 11 | 0 | 1 | 1 | 1 |
| 10 | 0 | 0 | 0 | 0 |

$$C = X_2X_3X_4 + \bar{X}_1\bar{X}_3X_4 + X_1X_3X_4$$

Implementing the logic circuit design using PLA




Question 2

i) There are 4 inputs to the circuit

∴ The number of states are $2^4$

= 16 states

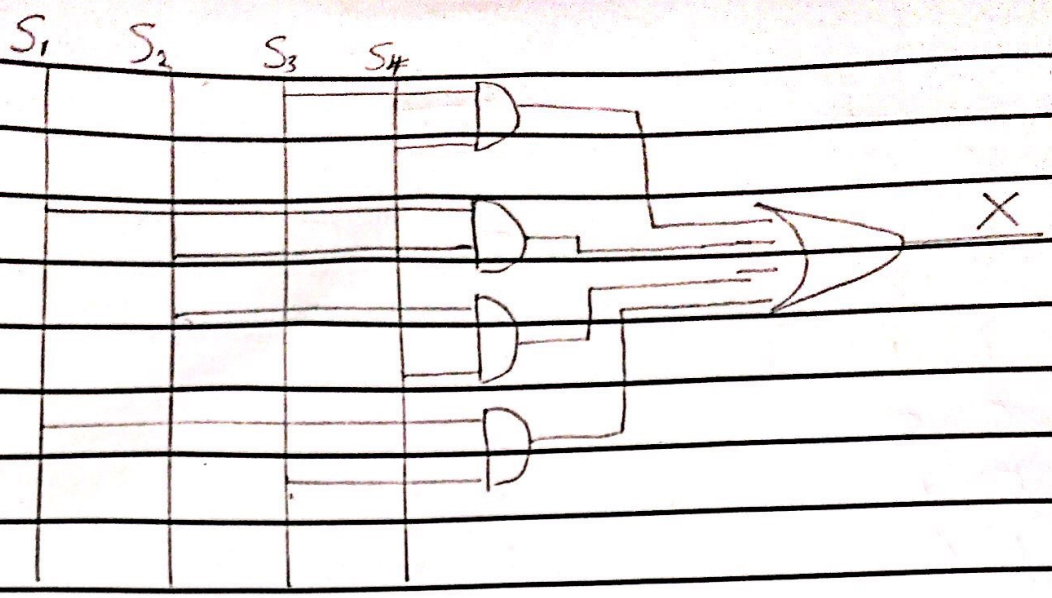
There are 4 switches [$S_1$ $S_2$ $S_3$ $S_4$]

Drawing the truth table

| $S_1$ | $S_2$ | $S_3$ | $S_4$ | X(Output) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | X(Don't care) |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | X(Don't care) |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | X(Don't care) |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | X(Don't care) |

| $S_3S_4$ \ $S_1S_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 1 | 0 |
| 01 | 1 | 1 | X | X |
| 11 | 1 | 1 | X | X |
| 10 | 0 | 1 | 1 | 1 |

$$X = S_3S_4 + S_1S_2 + S_2S_4 + S_1S_3$$




VHDL code:

```
library ieee;
Use ieee.std_logic_1164.all;
entity switches is
port (Sa, Sb, Sc, Sd : in
    std_logic; X: out std_logic);
end switches

Architecture dataflow of switches is
begin
  X <= (Sc and Sd) or
       (Sa and Sb) or
       (Sb and Sd) or
       (Sa and Sc);
end dataflow;
```