

OHADI JUNE-THADOLEVS

15/06/2020 COMPUTER ELG

CSE 506 ASSIGNMENT

(1) $A(x_1, x_2, x_3, x_4) = \sum m(3, 7, 8, 9, 11, 15)$

$B(x_1, x_2, x_3, x_4) = \sum m(3, 4, 5, 7, 10, 14, 15)$

$C(x_1, x_2, x_3, x_4) = \sum m(1, 5, 7, 11, 15)$

Truth table

x_1	x_2	x_3	x_4	A	B	C
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	0	0	0
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	1	0
1	1	1	1	1	1	1

Representation of the outputs in Boolean Expression

Output A :

$x_3 \backslash x_1 x_2$	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	1	1	1	1
10	0	0	0	0

$$A = x_1 \bar{x}_2 \bar{x}_3 + x_3 x_4$$

Output B :

$x_3 \backslash x_1 x_2$	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	1	1	1	0
10	0	0	1	1

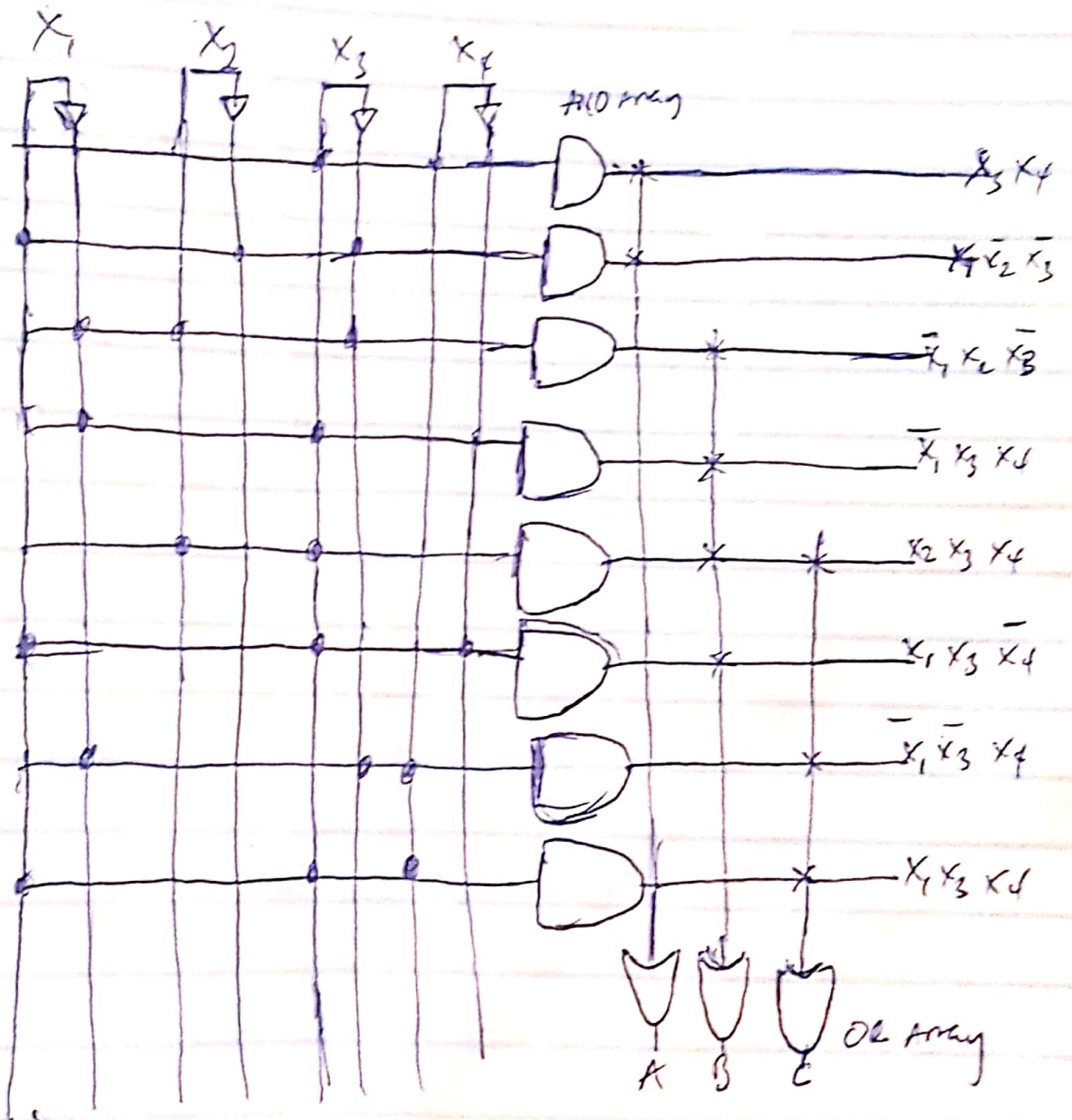
$$B = \bar{x}_1 \bar{x}_2 \bar{x}_3 + \bar{x}_1 x_3 x_4 + x_2 x_3 x_4 + x_1 x_3 \bar{x}_4$$

Output C :

$x_3 \backslash x_1 x_2$	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	0	1	1	1
10	0	0	0	0

$$C = \bar{x}_1 \bar{x}_3 x_4 + x_2 x_3 x_4 + x_1 x_3 \bar{x}_4$$

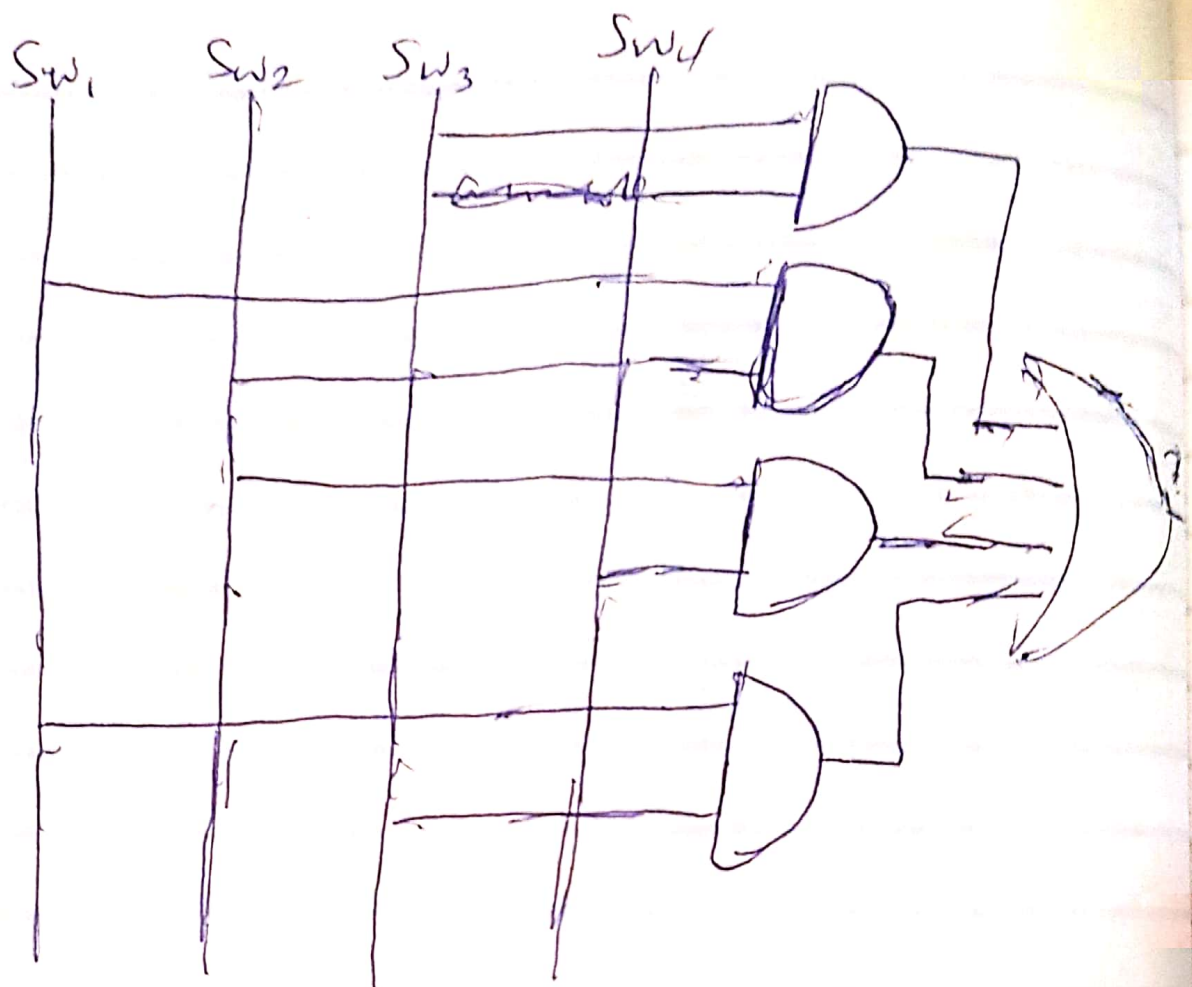
Logic circuit Design: Implementation using PLA



(2)

	S_{w1}	S_{w2}	S_{w3}	S_{w4}
0	0	1	0	
0	1	x	x	
1	1	x	x	
0	1	1	1	

$$X = S_{w3} S_{w4} + S_{w1} S_{w2} + S_{w2} S_{w4} + S_{w1} S_{w3}$$



Code:

Library ieee;

Use ieee std_logic_1164.all;

entity switches is

port (swa, swb, swc, swd) in std_logic; x out std_logic;

end switches

Architecture dataflow of switches

x <= (swc and swd) or

(swa and swb) or

(swb and swd) or

(swa and swc);

end dataflow;