15/ENG02/005
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COE506 Assignment

(1) $A(x_1\ x_2\ x_3\ x_4) = \sum m(3, 7, 8, 9, 11, 15)$

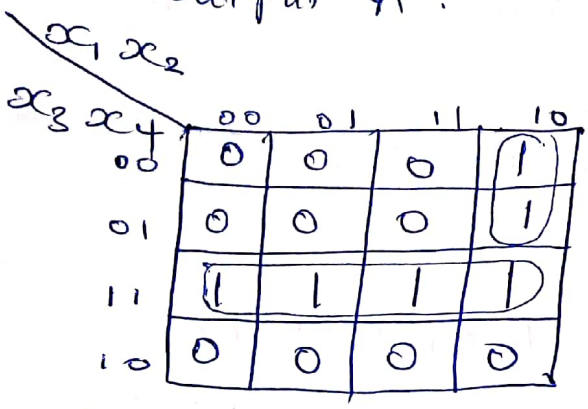
$B(x_1\ x_2\ x_3\ x_4) = \sum m(3, 4, 5, 7, 10, 14, 15)$

$C(x_1\ x_2\ x_3\ x_4) = \sum m(1, 5, 7, 11, 15)$

Truth table:

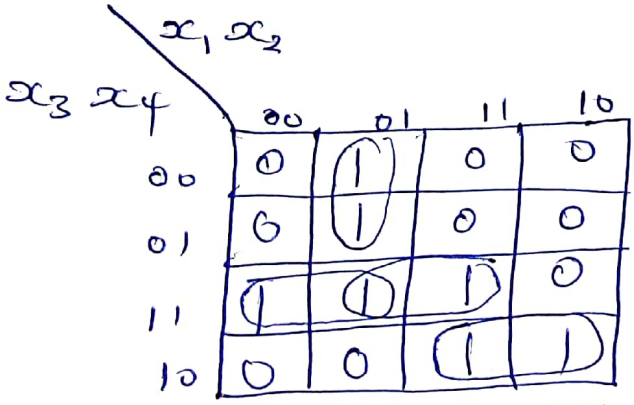
x_1	x_2	x_3	x_4	A	B	C
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	0	0	0
0	1	1	1	1	1	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	0	0	0
1	1	0	0	1	0	1
1	1	0	1	0	0	0
1	1	1	0	0	1	0
1	1	1	1	1	1	1

for output A:



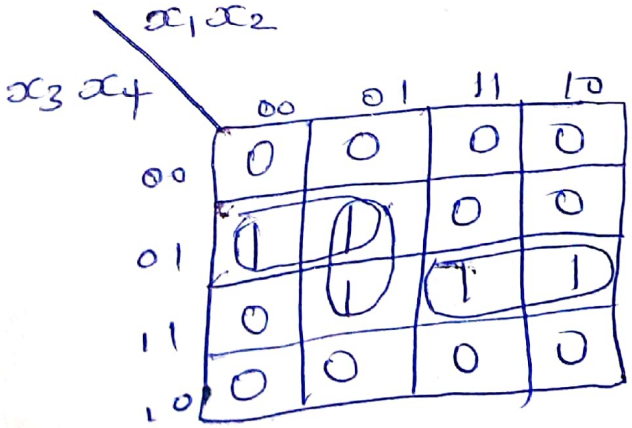
$$A = x_1 \bar{x_2} \bar{x_3} + x_3 x_4$$

for output B:



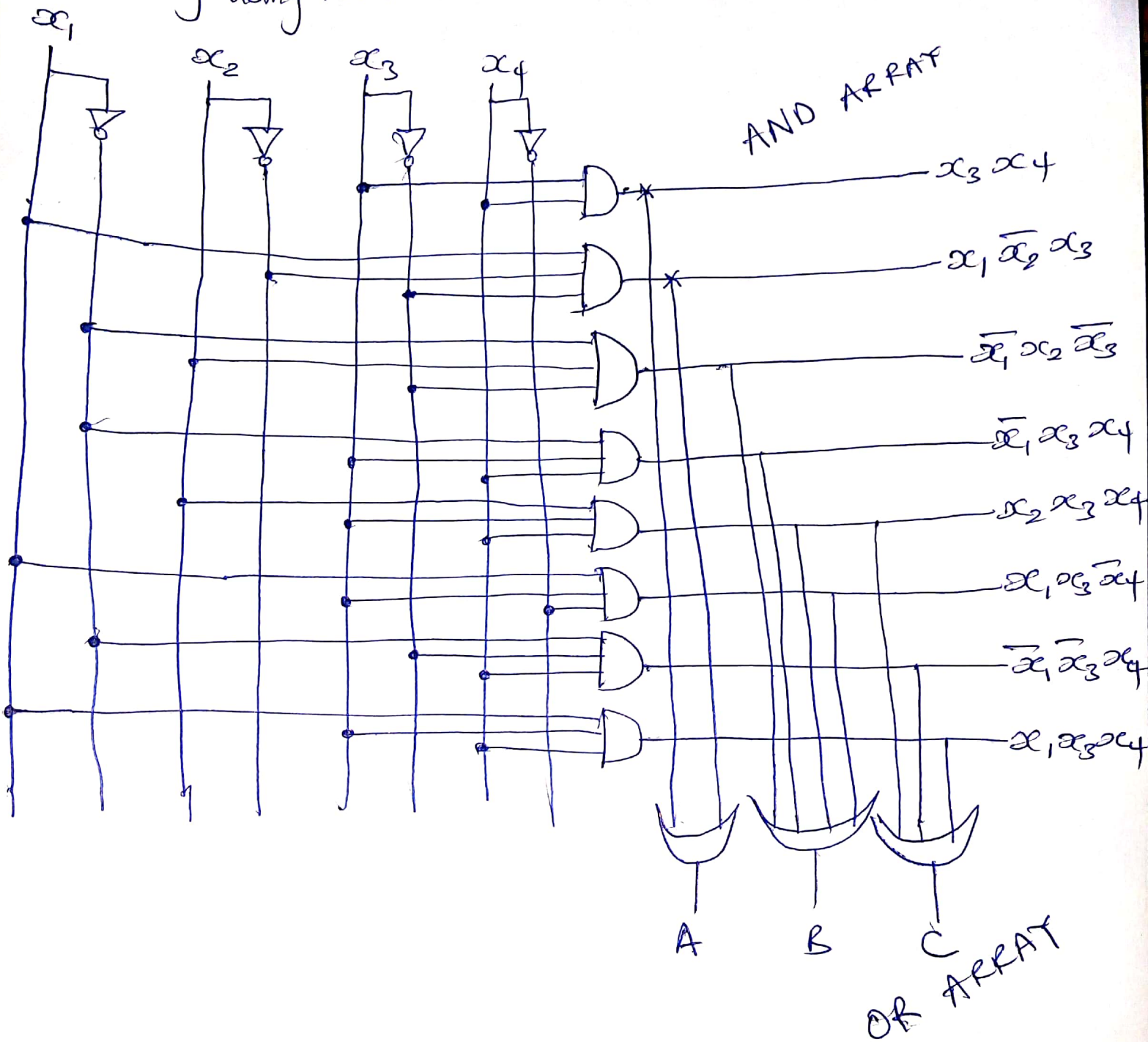
$$B = \bar{x_1} x_2 \bar{x_3} + \bar{x_1} x_3 x_4 + x_2 x_3 x_4 + x_1 x_3 \bar{x_4}$$

for output C:



$$C = \bar{x_1} \bar{x_3} x_4 + x_2 x_3 x_4 + x_1 x_3 x_4$$

Implementing using PLA;

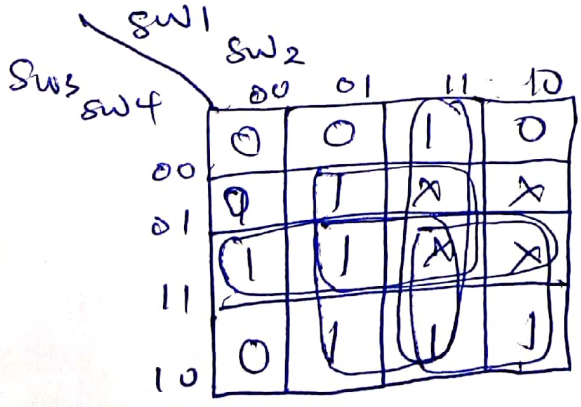


(2)

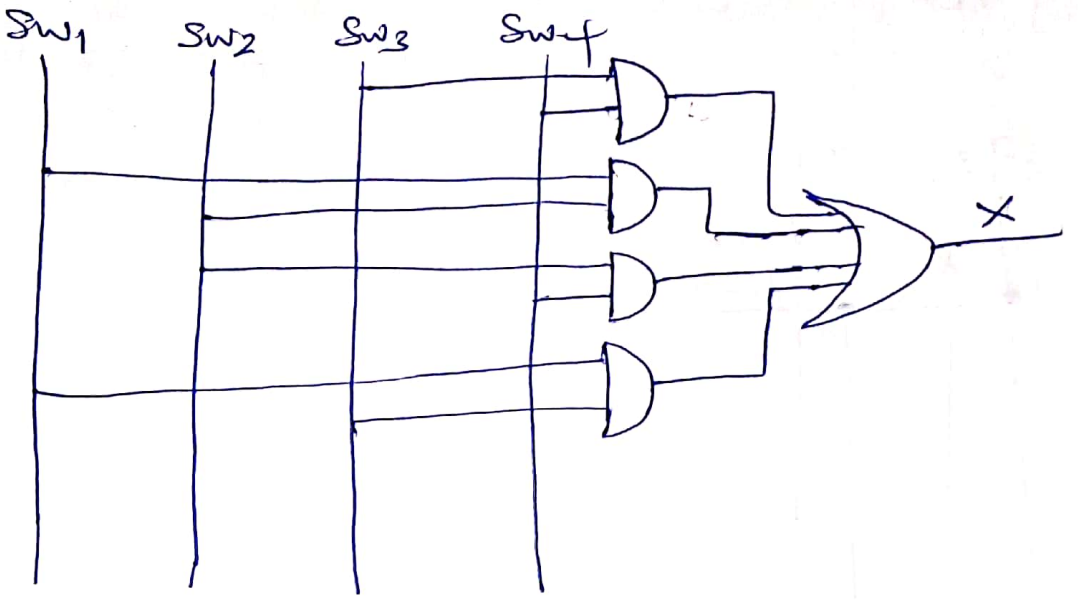
(i) from the logic circuit black box view, we have 4 inputs to the circuit : $2^4 = 16$ states

Truth table

SW1	SW2	SW3	SW4	x (output)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	X (don't care)
1	0	1	0	1
1	0	1	1	X (don't care)
1	1	0	0	1
1	1	0	1	X (don't care)
1	1	1	0	1
1	1	1	1	X (don't care)



$X = SW_3 SW_4 + SW_1 SW_2 + SW_2 SW_4 + SW_1 SW_3$



Code

```
library ieee;
use ieee.std_logic_1164.All ;
entity switches IS
Port(SWa, SWb, SWc, SWd : in
     std_logic; x: out std_logic);
end switches;
Architecture dataflow of switches IS
begin
  x <= (SWc and SWd) or
       (SWa and SWb) or
       (SWb and SWd) or
       (SWa and SWc) ;

end dataflow;
```