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15/ENG02/019

ASSIGNMENT 3

COE 506

1) $A(x_1\ x_2\ x_3\ x_4) = \Sigma m\ (3, 7, 8, 9, 11, 15)$

$B(x_1\ x_2, x_3\ x_4) = \Sigma m\ (3, 4, 5, 7, 10, 14, 15)$

$C(x_1\ x_2\ x_3\ x_4) = \Sigma m\ (1, 5, 7, 11, 15)$

Truth table;

	x_1	x_2	x_3	x_4	A	B	C
0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1
2	0	0	1	0	0	0	0
3	0	0	1	1	1	1	0
4	0	1	0	0	0	1	0
5	0	1	0	1	0	1	1
6	0	1	1	0	0	0	0
7	0	1	1	1	1	1	1
8	1	0	0	0	1	0	0
9	1	0	0	1	1	0	0
10	1	0	1	0	0	1	0
11	1	0	1	1	1	0	1
12	1	1	0	0	0	0	0
13	1	1	0	1	0	0	0
14	1	1	1	0	0	1	0
15	1	1	1	1	1	1	1

Boolean expression for A, B, C.

A;

X_3X_4 \ X_1X_2	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	1	1	1	1
10	0	0	0	0

$A = X_1\bar{X}_2\bar{X}_3 + X_3X_4$

B;

X_3X_4 \ X_1X_2	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	1	1	1	0
10	0	0	1	1

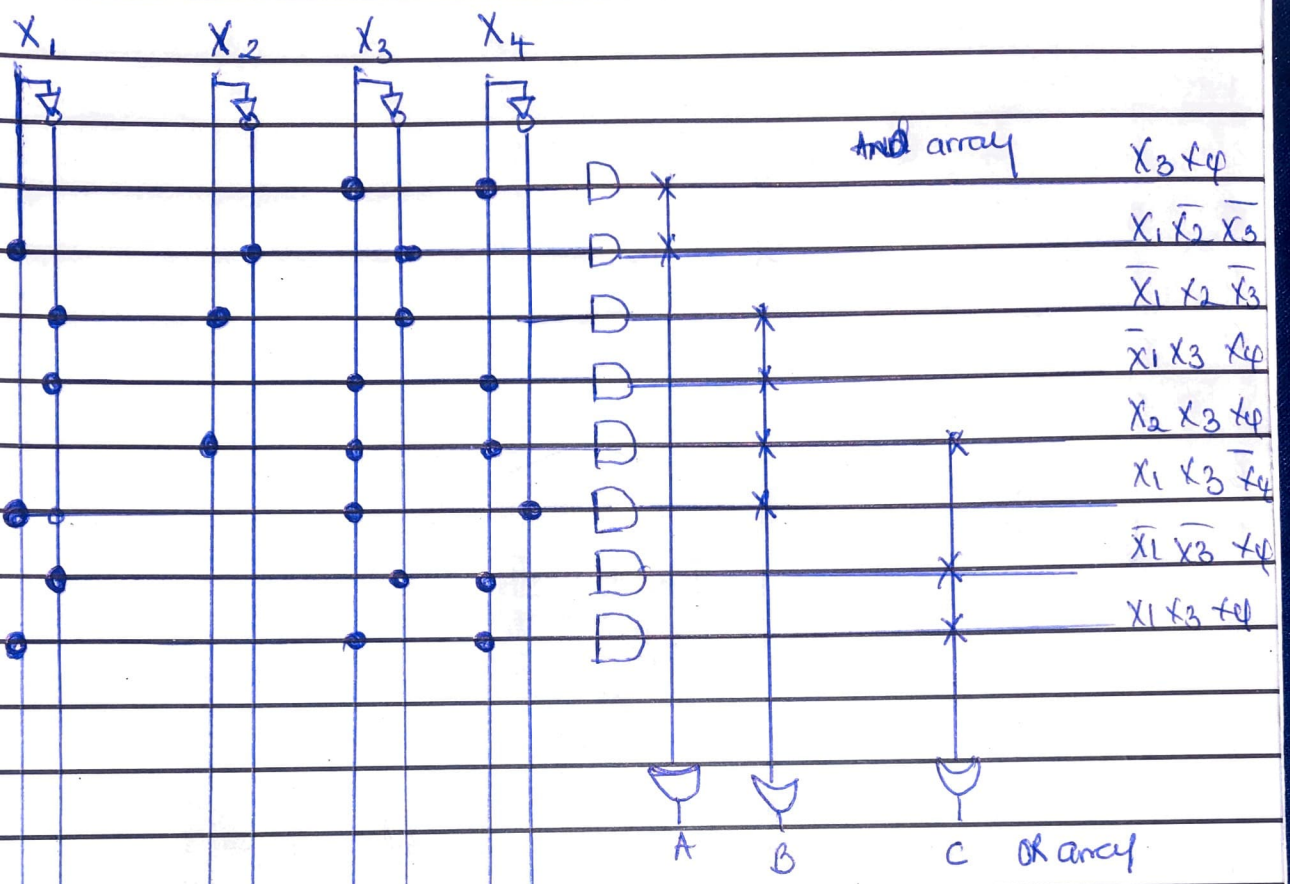
$B = \bar{X}_1X_2\bar{X}_3 + \bar{X}_1X_3X_4 + X_2X_3X_4 + X_1X_3\bar{X}_4$

C;

X_3X_4 \ X_1X_2	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	0	1	1	1
10	0	0	0	0

$C = \bar{X}_1\bar{X}_3X_4 + X_2X_3X_4 + X_1X_3X_4$

Logic circuit Design ; Implementing using PLA



2i) There are 4 inputs to the circuit, so:

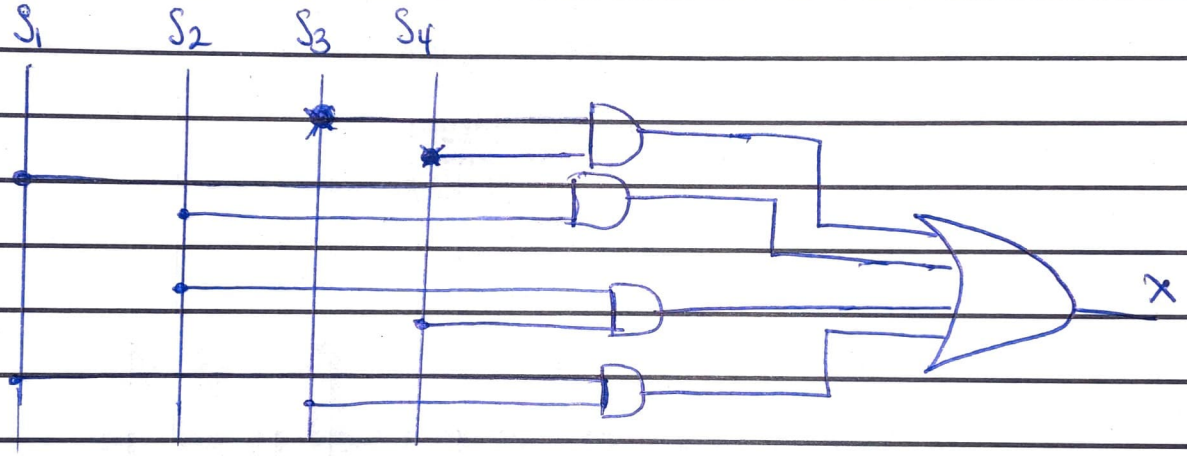
$2^4 = 16$ states.

Truth table

S_1	S_2	S_3	S_4	X (output)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	x (dont care)
1	0	1	0	1
1	0	1	1	x (dont care)
1	1	0	0	1
1	1	0	1	x (dont care)
1	1	1	0	1
1	1	1	1	x (dont care)

S_3S_4 \ S_1S_2	00	01	11	10
00	0	0	1	0
01	0	1	X	X
11	1	1	X	X
10	0	1	1	1

$X = S_3S_4 + S_1S_2 + S_2S_4 + S_1S_3$



Code;

```
library ieee;
use ieee.std_logic_1164.all;
entity switches is
Port (Sa, Sb, Sc, Sd : in
    std_logic; X : out std_
    logic );
    end switches;
    Architecture dataflow of switches is;
    begin
      X <= (Sc and Sd ) or
```

```
(sa and sb) or
(sb and sd) or
(sa and sc);

end data flow;
```