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15/ENG02/031

COE 506

ASSIGNMENT.

QUESTION ONE.

$A(X_1X_2X_3X_4) = \Sigma m(3,7,8,9,11,15)$

$B(X_1X_2X_3X_4) = \Sigma m(3,4,5,7,10,14,15)$

$C(X_1X_2X_3X_4) = \Sigma m(1,5,7,11,15)$

Truth Table

X_1	X_2	X_3	X_4	A	B	C
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	0	0	0
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	1	0
1	1	1	1	1	1	1

Boolean Representcon of the Outputs A, B and C

Output A:

X_3X_4 \ X_1X_2	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	1	1	1	1
10	0	0	0	0

$$A = X_1\bar{X}_2\bar{X}_3 + X_3X_4$$

Output B;

X_3X_4 \ X_1X_2	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	1	1	1	0
10	0	0	1	1

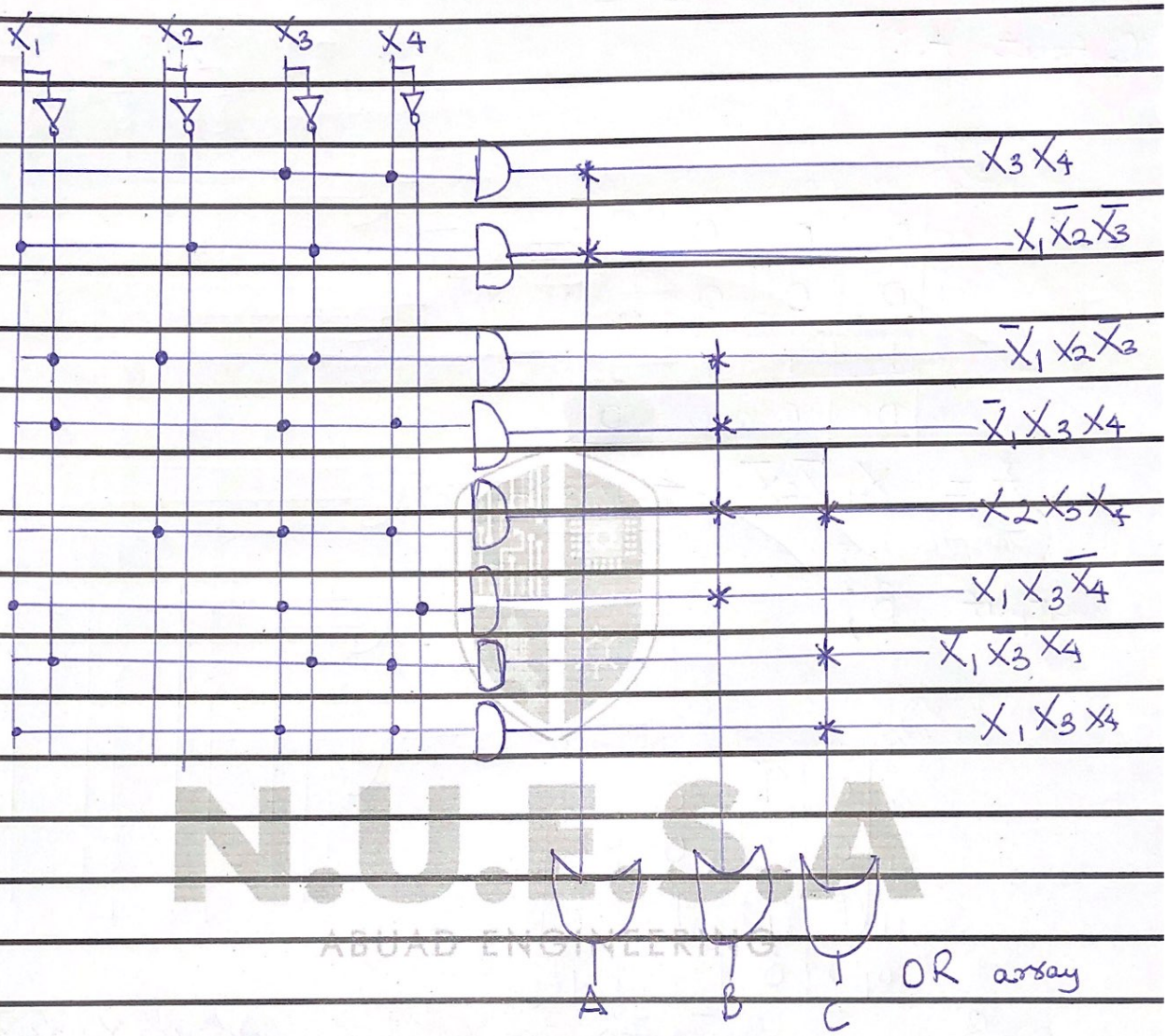
$$B = \bar{X}_1 X_2 \bar{X}_3 + \bar{X}_1 X_3 X_4 + X_2 X_3 X_4 + X_1 X_3 \bar{X}_4$$

Output C;

X_3X_4 \ X_1X_2	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	0	1	1	1
10	0	0	0	0

$$C = \bar{X}_1\bar{X}_3 X_4 + X_2 X_3 X_4 + X_1 X_3 X_4$$

Logic Circuit Design: Implementation Using PLA.



QUESTION TWO

(a) From the Logic Circuit black box Video we have 4 inputs to the Circuit

$2^4 = 16$ States.

Truth Table

SW_1	SW_2	SW_3	SW_4	X (output)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	X (Don't Care)
1	0	1	0	1
1	0	1	1	X (Don't Care)
1	1	0	0	1
1	1	0	1	X (Don't Care)
1	1	1	0	1
1	1	1	1	X (Don't Care)

11) Behavioural VHDL model for the minimized Boolean expression

In this Code we could represent the following;

$SW1 = a$
$SW2 = b$
$SW3 = C$
$SW4 = d$

} Input

$X = X \rightarrow$ Output

Code:

```
library ieee;
Use ieee.Std_Logic_1164.all;
entity Switches is
port (Sw_a, Sw_b, Sw_c, Sw_d : in
 Std_Logic; X: Out Std_
 Logic);

end Switches

Architecture data flow of Switches is
begin
 X <= ((Sw_c and Sw_d) or
      (Sw_a and Sw_b) or
      (Sw_b and Sw_d) or
      (Sw_a and Sw_c));
end data flow;
```

iii) K-map

Sw_3Sw_4 \ Sw_1Sw_2	00	01	11	10
00	0	0	1	0
01	0	1	X	X
11	1	1	X	X
10	0	1	1	1

$X = Sw_3Sw_4 + Sw_1Sw_2 + Sw_2Sw_4 + Sw_1Sw_3.$

Logic Circuit Design.