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15/ENG02/036
COE 506

(1) A $(x_1\ x_2\ x_3\ x_4)$ = $\Sigma m\ (3, 7, 8, 9, 11, 15)$
B $(x_1\ x_2\ x_3\ x_4)$ = $\Sigma m\ (3, 4, 5, 7, 10, 14, 15)$
C $(x_1\ x_2\ x_3\ x_4)$ = $\Sigma m\ (1, 5, 7, 11, 15)$

TRUTH TABLE

x_1	x_2	x_3	x_4	A	B	C
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	0	0	0
0	1	1	1	0	1	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	0
1	1	1	0	0	1	0
1	1	1	1	1	1	1

Output A:

x_3x_4 \ x_1x_2	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	1	1	1	1
10	0	0	0	0

$A = x_1\bar{x}_2\bar{x}_3 + x_3x_4$

Output B:

x_3x_4 \ x_1x_2	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	1	1	1	0
10	0	0	1	1

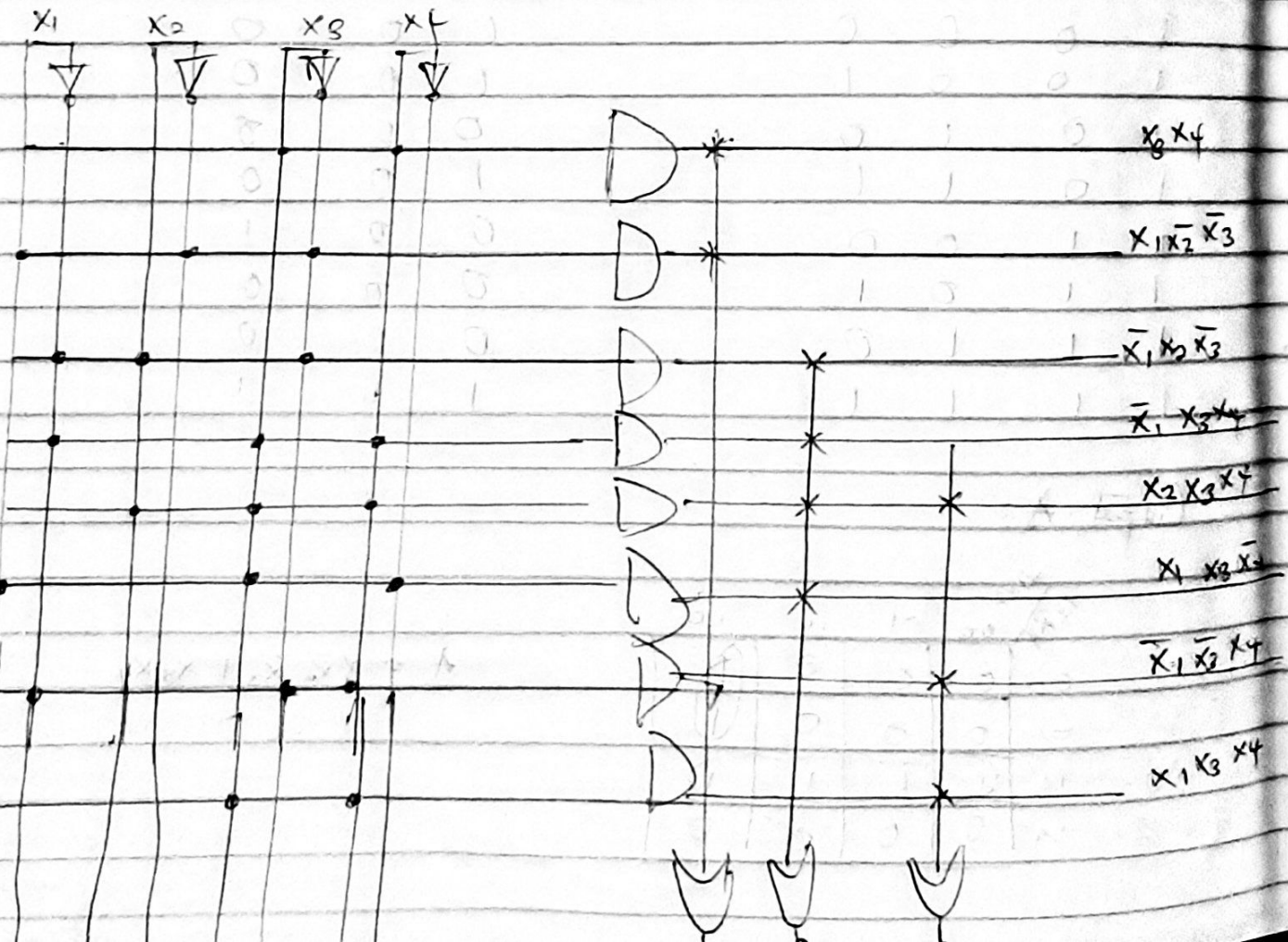
$B = \bar{x}_1 x_2 \bar{x}_3 + \bar{x}_1 x_3 x_4 + x_2 x_3 x_4 + x_1 x_3 \bar{x}_4$

Output C:

x_3x_4 \ x_1x_2	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	0	1	1	1
10	0	0	0	0

$C = \bar{x}_1 \bar{x}_3 x_4 + x_2 x_3 x_4 + x_1 x_3 \bar{x}_4$

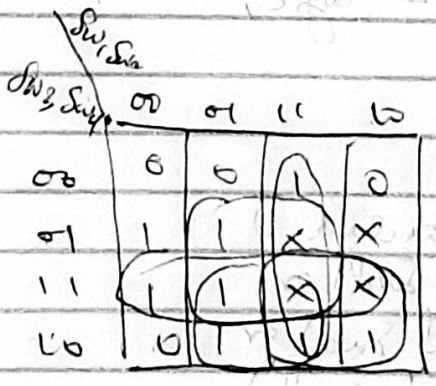
Logic Circuit Design:



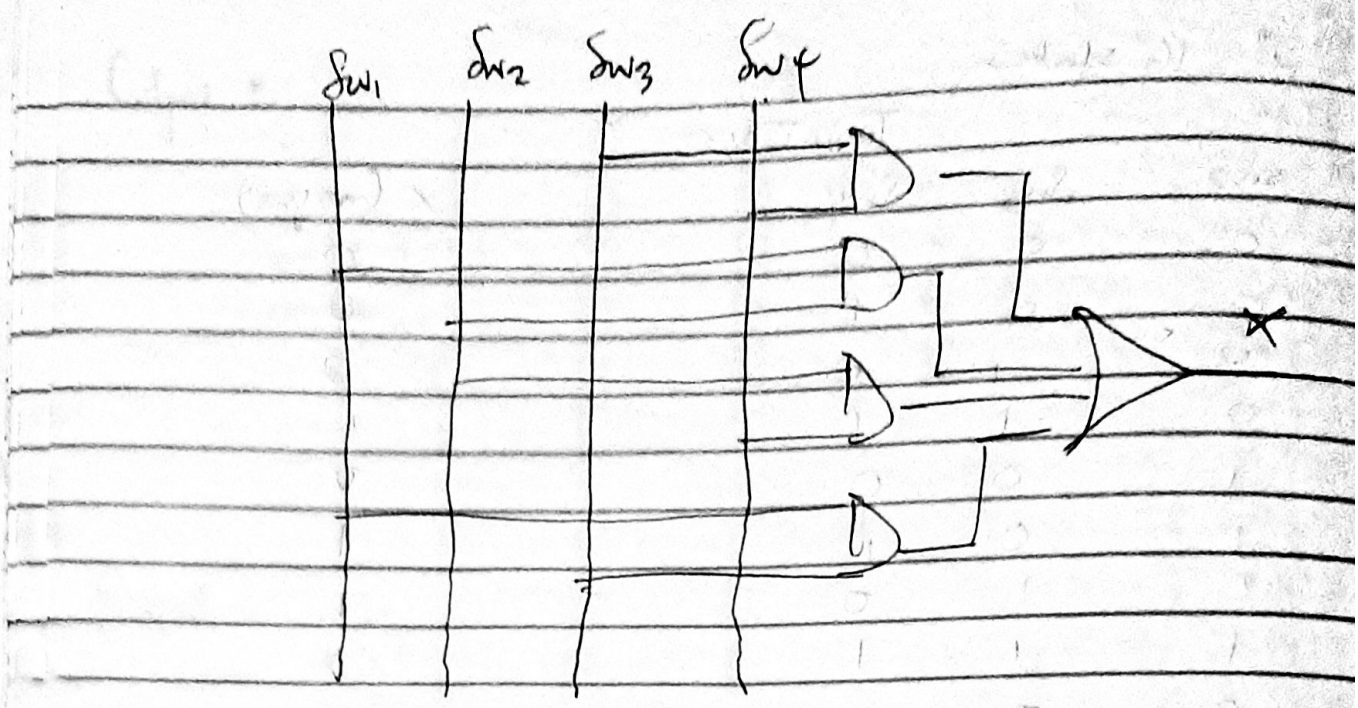
(2) (i) $2^4 = 16$ states

TRUTH TABLE:

sw_1	sw_2	sw_3	sw_4	x (output)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	X
1	0	1	0	1
1	0	1	1	X
1	1	0	0	1
1	1	0	1	X
1	1	1	0	1
1	1	1	1	X



$$x = sw_3 sw_4 + sw_1 sw_2 + sw_2 sw_4 + sw_1 sw_3$$



Code:

```
library ieee;
Use ieee.std_logic_1164;
entity switches is
Port sw_a, sw_b, sw_c, sw_d: in
  std_logic; x: out std_logic;

end switches.

Architecture dataflow of switches is
begin  x <= (sw_c and sw_d) or
            (sw_a and sw_b) or
            (sw_b and sw_d) or
            (sw_a and sw_c);

end data flow;
```