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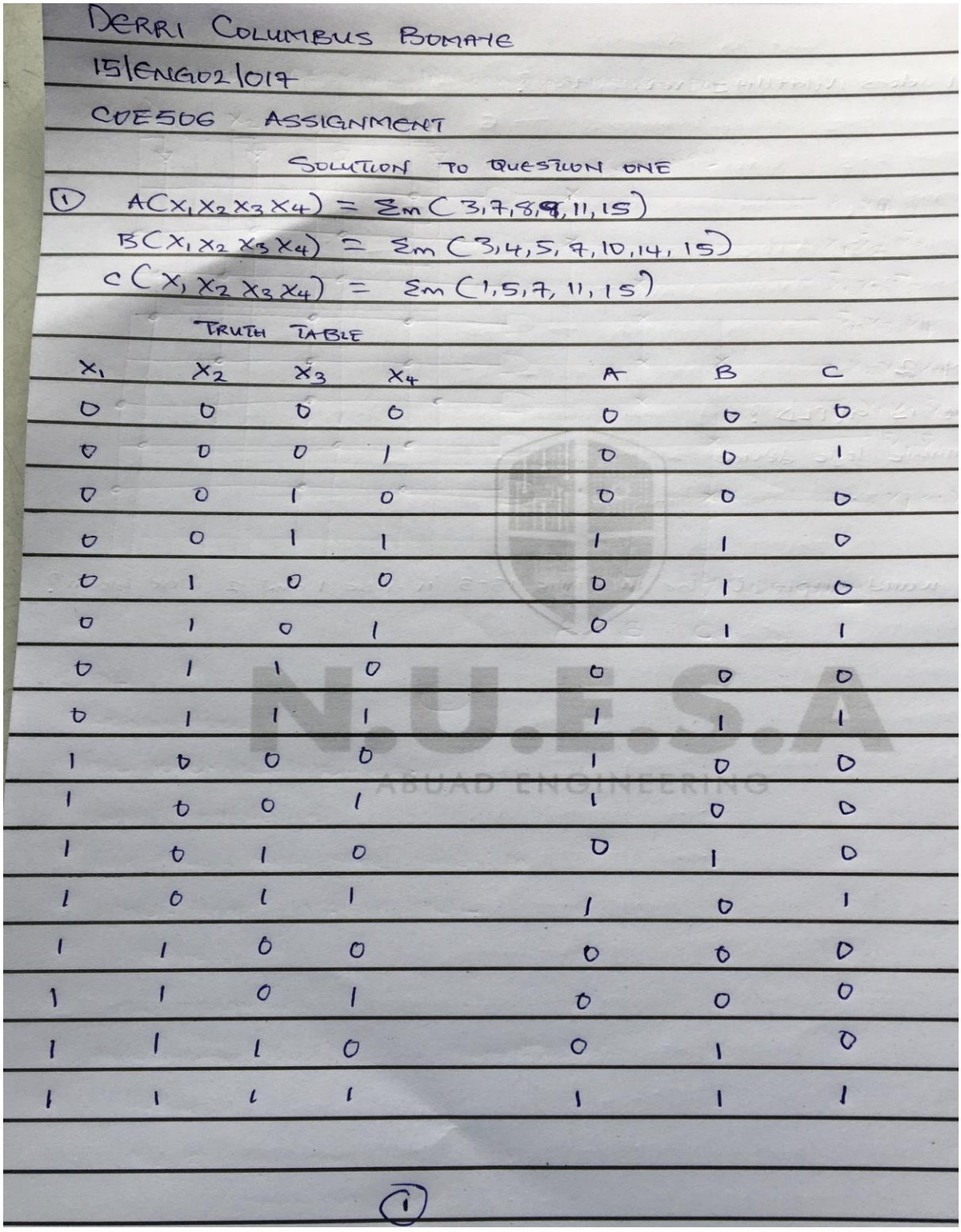
MATRIC NO: 15/ENG02/017

DEPT: COMPUTER ENGINEERING

COURSE CODE: COE506

COURSE TITLE: DIGITAL DESIGN USING VHDL



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COE506 ASSIGNMENT

SOLUTION TO QUESTION ONE

(1) $A(X_1 X_2 X_3 X_4) = \Sigma m(3,7,8,9,11,15)$

$B(X_1 X_2 X_3 X_4) = \Sigma m(3,4,5,7,10,14,15)$

$C(X_1 X_2 X_3 X_4) = \Sigma m(1,5,7,11,15)$

TRUTH TABLE

X_1	X_2	X_3	X_4	A	B	C
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	1	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	0	0	0
0	1	1	1	1	1	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	1	0
1	1	1	1	1	1	1

(1)

Boolean representation of the outputs A, B, and C

Output A:

x_3x_4 \ x_1x_2	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	1	1	1	1
10	0	0	0	0

$$A = x_1 \bar{x}_2 \bar{x}_3 + x_3 x_4$$

Output B:

x_3x_4 \ x_1x_2	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	1	1	1	0
10	0	0	1	1

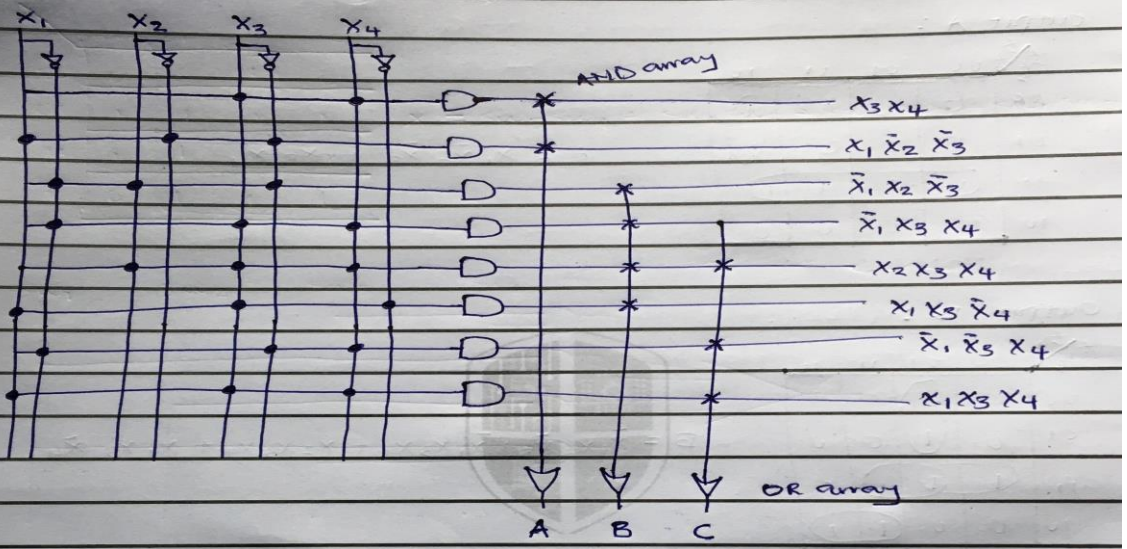
$$B = \bar{x}_1 x_2 \bar{x}_3 + \bar{x}_1 x_3 x_4 + x_2 x_3 x_4 + x_1 x_3 \bar{x}_4$$

Output C:

x_3x_4 \ x_1x_2	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	0	1	1	1
10	0	0	0	0

$$C = \bar{x}_1 \bar{x}_3 x_4 + x_2 x_3 x_4 + x_1 x_3 x_4$$

LOGIC CIRCUIT DESIGN: IMPLEMENTING USING PLA



QUESTION TWO SOLUTION

(2i) From the logic circuit below Black box view we have 4 inputs to the circuit.

$2^4 = 16$ states

TRUTH TABLE

SW_1	SW_2	SW_3	SW_4	X (OUTPUT)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	X
1	0	1	0	1
1	0	1	1	X
1	1	0	0	1
1	1	0	1	X
1	1	1	0	1
1	1	1	1	X

Boolean Expression : using K-map

SW_3SW_4 \ SW_1SW_2	00	01	11	10
00	0	0	1	0
01	1	1	x	x
11	1	1	x	x
10	0	1	1	1

$X = SW_3SW_4 + SW_1SW_2 + SW_2SW_4 + SW_1SW_3$

CODE :

```
Library ieee;
use ieee.std_logic_1164.all;
Entity switches is
Port swa, swb, swc, swd : in
 Std_logic ; x : out Std_
  logic) ;
 End switches
Architecture dataflow of switches is
 begin
x <= (swc and swd) or
     (swa and swb) or
     (swb and swd) or
     (swa and swc) ;
end data flow;
```